COMPACT DISC AUTO CHANGER

KDC-C100

SERVICE MANUAL

KENWOOD

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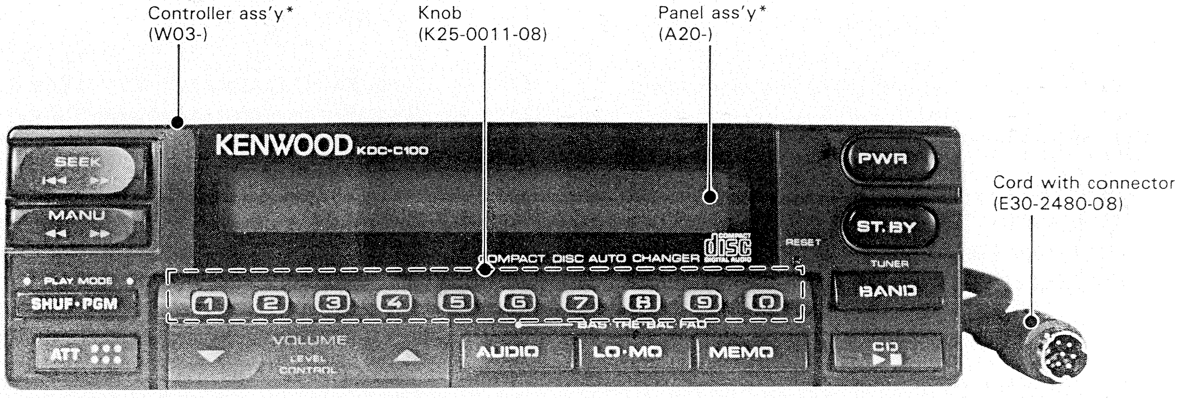
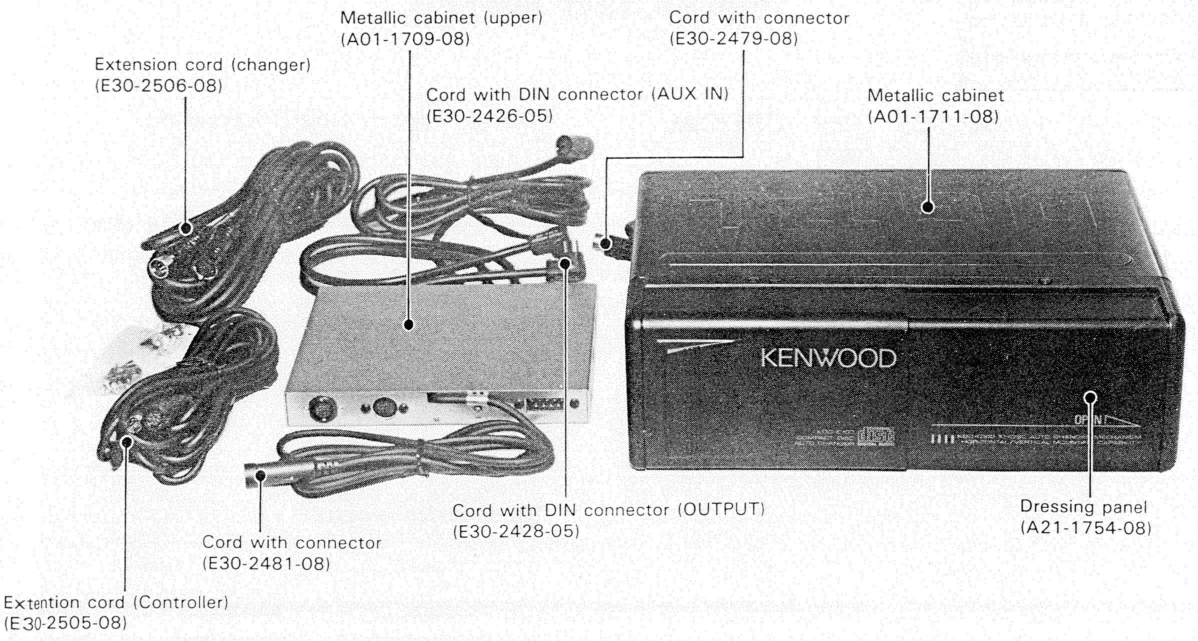
B51-3544-00(T)2531


Controller ass'y*
(W03-)
Knob
(K25-0011-08)
Panel ass'y*
(A20-)
Cord with connector
(E30-2480-08)
KENWOOD KDC-C100
SEEK
MANU
PLAY MODE
SHUF·PGM
ATT
COMPACT DISC AUTO CHANGER
RESET
PWR
ST.BY
TUNER
BAND
VOLUME
LEVEL
CONTROL
AUDIO
LO·MO
MEMO
CD
BAS TRE BAL FAD
1
2
3
4
5
6
7
8
9
0


Metallic cabinet (upper)
(A01-1709-08)
Cord with connector
(E30-2479-08)
Extension cord (changer)
(E30-2506-08)
Cord with DIN connector (AUX IN)
(E30-2426-05)
Metallic cabinet
(A01-1711-08)
KENWOOD
OPEN
Dressing panel
(A21-1754-08)
Cord with DIN connector (OUTPUT)
(E30-2428-05)
Cord with connector
(E30-2481-08)
Extention cord (Controller)
(E30-2505-08)

CAUTION
Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Precaution for servicing
The KDC-C100 is composed of a set of three components; the controller, hide-away unit and changer. As every single trouble could be due to one, some or all of these three components, all of them must be present when servicing or checking the KDC-C100.

* Refer to parts list on page 88.

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SERVICING NOTES

NOTES ON HANDLING THE OPTICAL PICK-UP BLOCK OR BASE UNIT

The laser diode in the optical pick-up block may suffer electrostatic breakdown because of the potential difference generated by the charged electrostatic load, etc. on clothing and the human body.

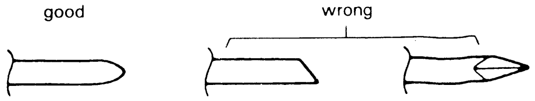
During repair, pay attention to electrostatic breakdown and also use the procedure in the printed matter which is included in the repair parts.

The flexible board is easily damaged and should be handled with care.

Flexible Circuit Board Repairing

1. Keep the temperature of the soldering iron at 270° ±10°C during repairing.
   You can maintain the temperature of the soldering iron around 270°C by using the thermal controller as illustrated on the right.
2. Do not touch the soldering iron more than 4 seconds or 3 times on the same conductor of the circuit board.
3. Do not apply force on the conductor when soldering or unsoldering.

Tip of soldering iron



CONTROLS AND INDICATORS

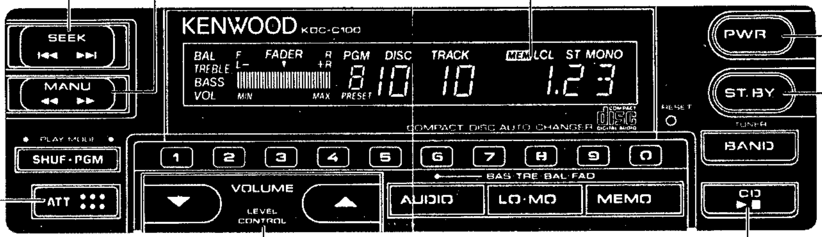
[CD]: Switch function or display during Compact Disc player operation.
[TUNER]: Swtich function or display during tuner operation. (When the optional KTC-T100 is used.)

[CD]: Music search switches
During CD play, press either side of this switch to start playback at the beginning of a particular selection.
⏮: To go back to the beginning of a previous selection.
⏭: To skip ahead to the beginning of a later selection.
[TUNER]: Seek tuning switches
Press ⏭ switch for up seek operation.
Press ⏮ switch for down seek operation.
Seek operation automatically stops when a marginal broadcast is received.

[CD]: Search switches
During CD play, press either side of this switch to search for a particular point on the disc.
◀◀: To go backwards at high speed.
▶▶: To skip ahead at high speed.
[TUNER]: Manual tuning switches
Press this switch once to change the receiving frequency by one step. When this switch is kept pressed, the frequency changes continuously.

Display window
Normally indicates the volume level. When adjusting the Bass, Treble, Balance or Fader control, it shows the corresponding adjustment level.
[CD]: Indicates the Disc No., Track No., playback time and the Program No. ''LOAD'' will be shown when changing discs.
[TUNER]: Indicates the selected Band, receiving frequency, and Preset No. ''ST'' will be shown when a stereo broadcast is being received.

Power switch
Turns the power of this unit ON and OFF.


SEEK
MANU
KENWOOD KDC-C100
BAL
TREBLE
BASS
VOL
F FADER R
L− +R
MIN MAX
PGM
PRESET
DISC
TRACK
MEMO LCL
ST MONO
8 10 10 1.23
COMPACT DISC AUTO CHANGER
COMPACT disc DIGITAL AUDIO
RESET
PWR
ST.BY
TUNER
BAND
CD
PLAY MODE
SHUF·PGM
ATT
1 2 3 4 5 6 7 8 9 0
BAS TRE BAL FAD
VOLUME
LEVEL CONTROL
AUDIO
LO·MO
MEMO

Attenuator switch
When this switch is ON, the indicator lights and the volume instantaneously drops. When this switch is pressed again, the indicator goes off and the previous volume resumes.

Volume up (▲)/down (▼) switch
Used for volume adjustment. These switches are also used to adjust the Bass, Treble, Balance and Fader.

[CD]: CD switch
Press this switch to start disc play. When it is pressed during play, disc play is suspended at the current position. Pressing it again resumes disc play from the same position. This switch is also used to select the disc to be played.

Stand-by switch
When this switch is pressed, the playing disc or the tuner (KTC-T100) will be turned OFF, and the sound from the component connected to the AUX input jacks can be heard (except some components).

CONTROLS AND INDICATORS

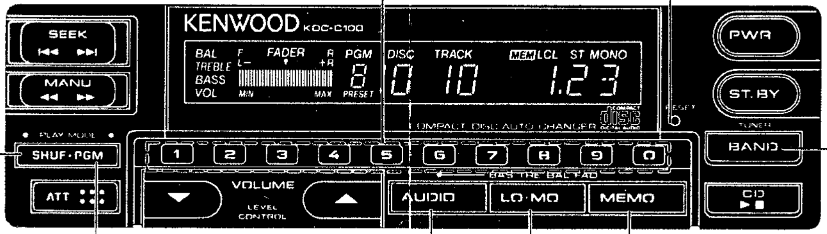
[CD]: Switch function or display during Compact Disc player operation.
[TUNER]: Swtich function or display during tuner operation. (When the optional KTC-T100 is used.)

[CD] : Shuffle switch
When this switch is pressed, shuffle play (playing the selections in a random order) starts.

[CD]: Preset program switches (1 — 0)
Each of these switches can store one of the selections contained on a disc, specified by the Disc No. and Track No.
[TUNER]: Preset station switches (1 — 0)
One switch can memorize one of each FM and AM.

Reset button
When the installation and all the wiring is finished, press this button. Not usually used however, when the microprocessor (micro-computer) malfunctions, press this button using a sharp-pointed object. When this button is pressed, the unit is reset to its initial state. Therefore, all the memories and clock needs to be adjusted.

[TUNER] : Band switch
With the tuner OFF, pressing this switch turns the tuner ON. With the tuner ON, the switch is used to select the reception band.


SEEK
MANU
PLAY MODE
SHUF·PGM
ATT
KENWOOD KDC-C100
BAL F FADER R PGM
TREBLE L— +R
BASS
VOL MIN MAX PRESET
DISC TRACK
MEM LCL ST MONO
COMPACT DISC AUTO CHANGER
RESET
1
2
3
4
5
6
7
8
9
0
BAS TRE BAL FAD
VOLUME
LEVEL CONTROL
AUDIO
LO·MO
MEMO
PWR
ST.BY
TUNER
BAND
CD

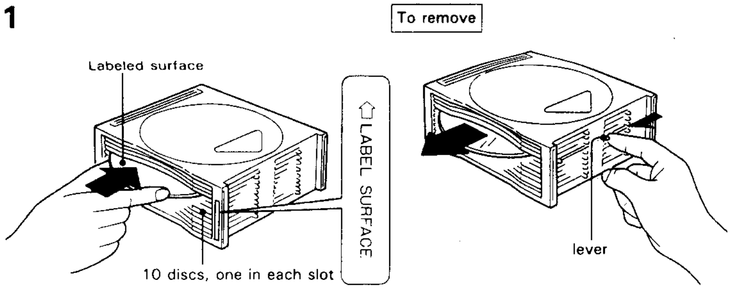
[CD]: Program switch
When this switch is pressed, the programmed selections (specified by the Disc No. and Track No.) will be played.

Audio switch
When this switch is pressed, the Bass, Treble, Balance or Fader can be adjusted using the ▲ / ▼ switch.

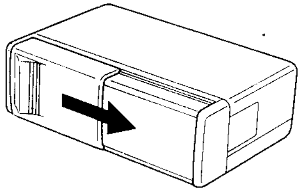
[TUNER] : Local/Mono switch
This switch selects Local mode only when a strong signal station is received. It selects Monaural mode when FM reception is noisy.

[CD] : Memory switch
Press this switch to memorize the disc or track for a Preset program switch.
[TUNER]: Memory switch
Press this switch to memorize the frequency during radio reception.

1



2



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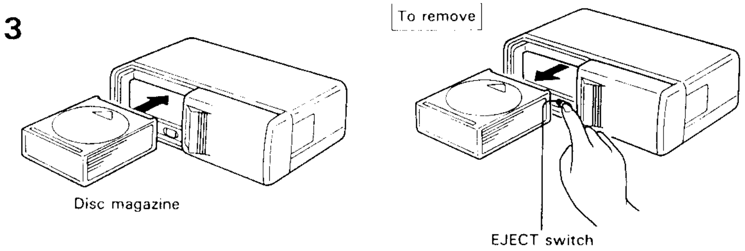

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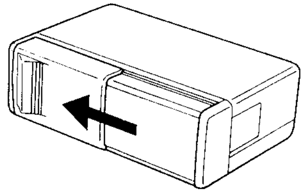


Use the unit with the door closed

Otherwise, foreign matter may enter the unit, and contaminate the lens in the player.

■ Disc play

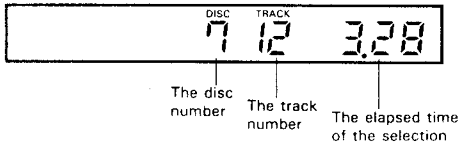
1. Turn the power ON.
2. Set the compact discs in the disc magazine, and load the magazine to the changer.
3. Press the CD switch. disc play starts.
4. Adjust the Volume, Bass, Treble, Balance and Fader controls as required.

Note:

When the volume up (▲) switch is held pressed, the volume is increased to a fixed level, then the incrementing stops. To further increase the volume, release the switch, and then press it again.

5. To place the CD changer in pause mode, press the CD switch. Pressing the CD switch again releases pause mode.
6. To stop disc play, press the Stand-by switch. When the Stand-by switch is pressed, the sound from the component connected to the AUX input jacks is heard (except some components).
7. To recall a required disc in the magazine, press the corresponding Disc No. of the Preset program switches, then within 5 seconds, press the CD switch. While the disc is being changed, "LOAD" is shown in the display window.
8. To recall a required track, press the Track No. of the Preset program switches, then within 5 seconds, press the Music search switch.

Display window



NOTE

At the end of the disc

When disc reaches the end of the last selection of the disc, play of the next disc starts automatically. At the end of the last disc, the unit will go back to the beginning of the first disc, and the play will restart.

When no disc is in the changer

- When the CD switch is pressed without the disc magazine in the changer, [E-01] is displayed. Insert the disc magazine into the changer and press the CD switch.
- When the CD switch is pressed with no disc in the disc magazine, [E-02] is displayed. Insert the disc into the disc magazine and press the CD switch.

When the tuner is connected

The disc play also stops when the Band switch is pressed. To restart disc play, press the CD switch. Play will start from the point at which play was stopped.

This unit will automatically start playing in the following case

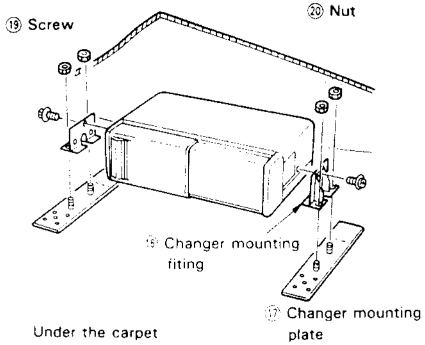
If the car ignition key is turned off during play and turned to the IGN (ignition) or ACC (accessory) position again within 32 seconds, the unit will restart the play from the same point. If the key is turned to the IGN (ignition) or ACC (accessory) position again after 32 seconds, the unit will restart from the beginning of the selection that was being played.

Mounting diagram 1

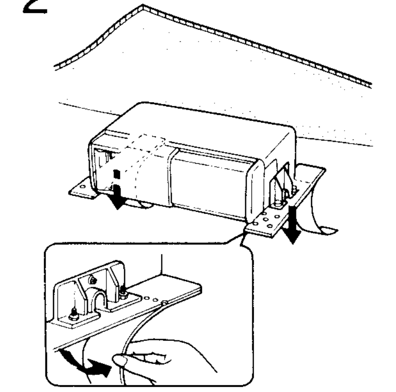
* If the installation is not secure, sound skipping may occur. For secure installation, proceed the Mounting diagram 2.

Horizontal

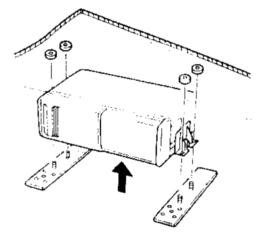
1 Place the holes of the changer mounting fitting ⑯ upon the protrusions on the bottom of the main unit.


⑲ Screw
⑳ Nut
⑯ Changer mounting fiting
⑰ Changer mounting plate
Under the carpet

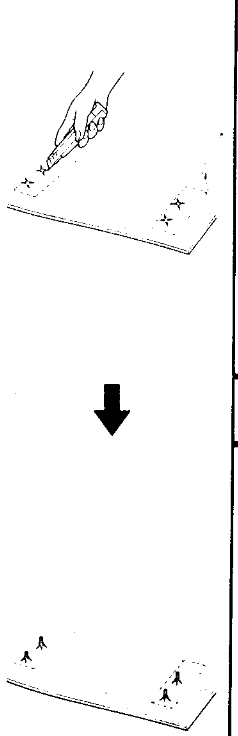
2



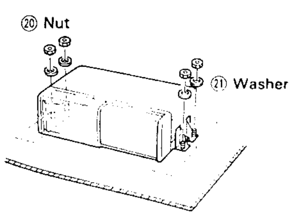
3 Detach the unit only.



4

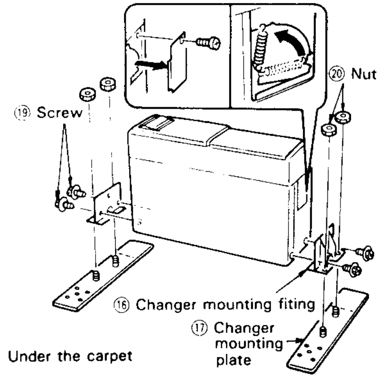


5

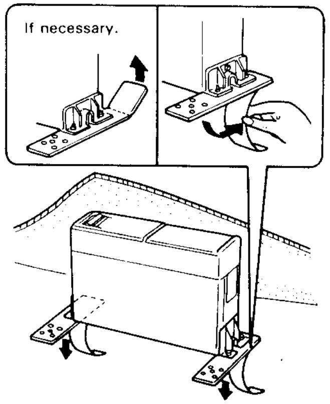

⑳ Nut
㉑ Washer

Vertical

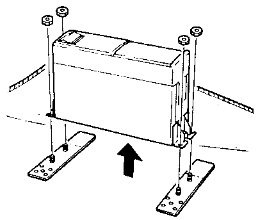
1 Remove the springs on both sides of the main unit, and hang them again (as shown in the figure).


⑳ Nut
⑲ Screw
⑯ Changer mounting fiting
⑰ Changer mounting plate
Under the carpet

2


If necessary.

3 Detach the unit only.



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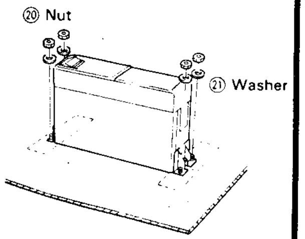
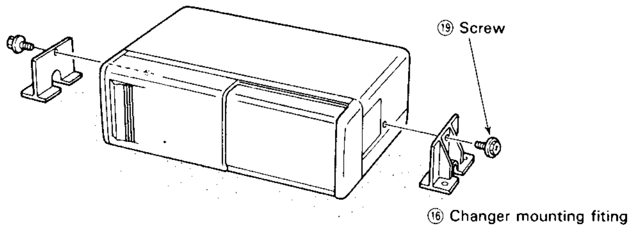

⑳ Nut
㉑ Washer

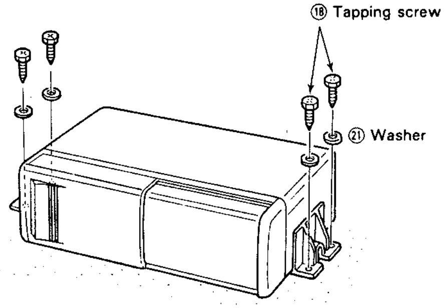
Mounting diagram 2

Horizontal

1 Place the holes of the changer mounting fitting ⑯ upon the protrusions on the bottom of the main unit.

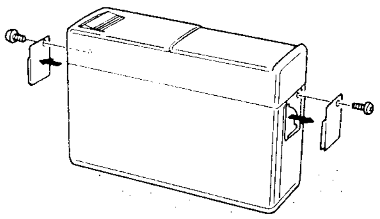

⑲ Screw
⑯ Changer mounting fitting

2 Drill bolt holes approx. 4 mm in diameter.

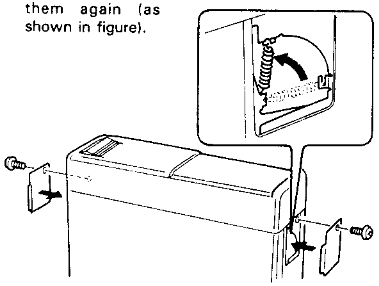

⑱ Tapping screw
㉑ Washer

Vertical

1



2 Remove the springs on both sides of the main unit, and hang them again (as shown in figure).



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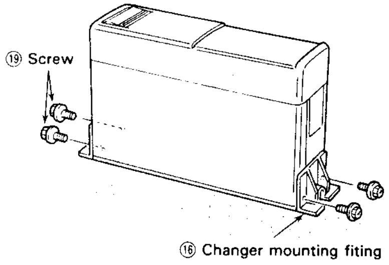
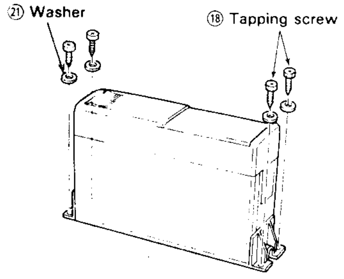

⑲ Screw
⑯ Changer mounting fiting

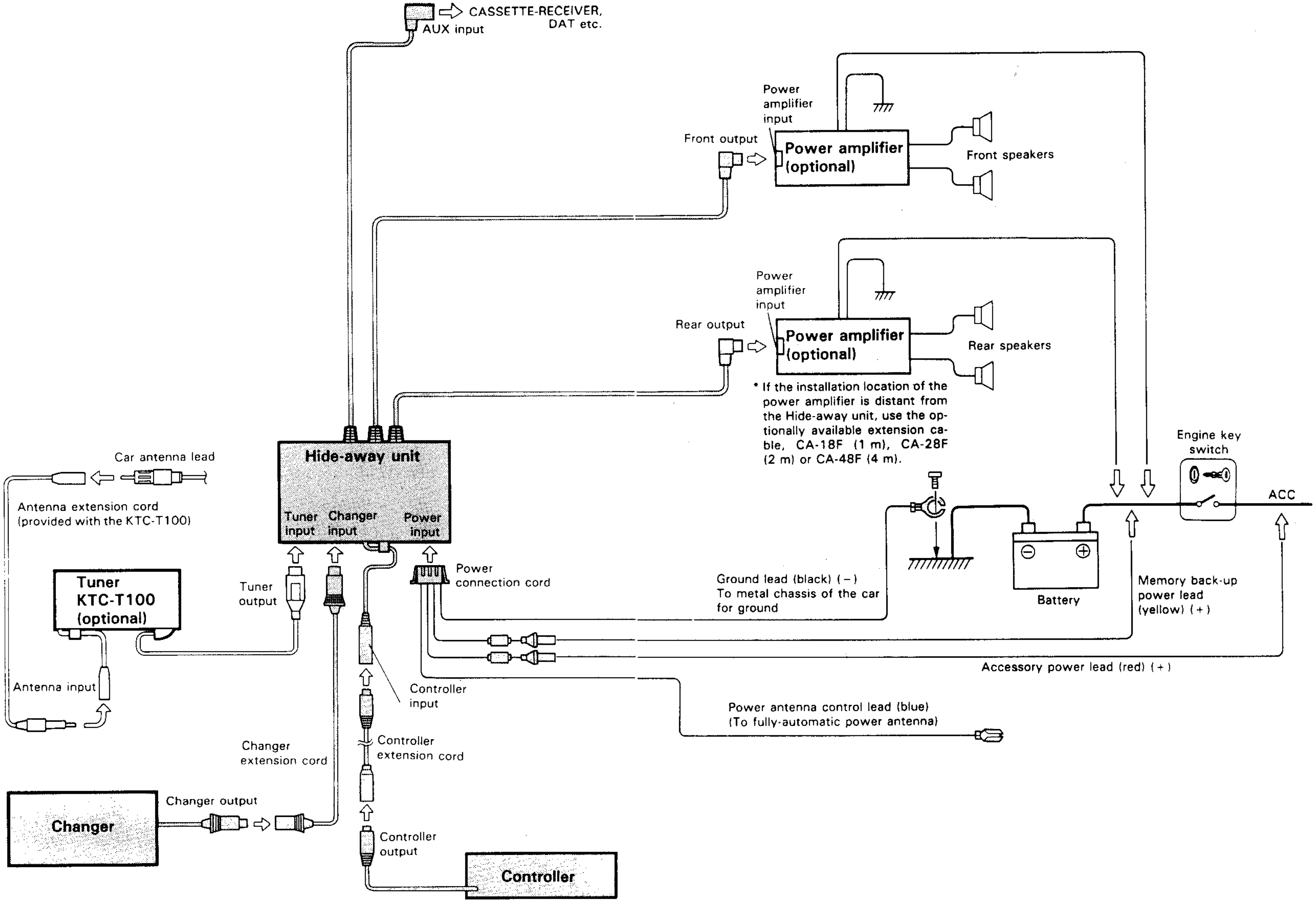
4 Drill bolt holes approx. 4 mm in diameter.


㉑ Washer
⑱ Tapping screw

CAUTION

When making the hole, make sure not to damage the fuel tank, brake tube, wiring harnesses, etc. on the other side.

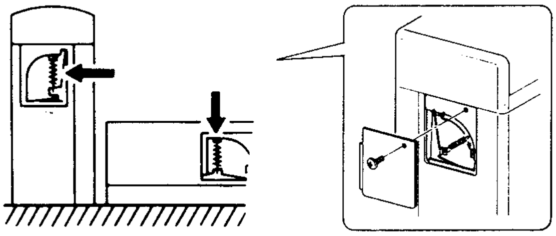
CONNECTION


CASSETTE-RECEIVER, DAT etc.
AUX input
Power amplifier input
Front output
Power amplifier (optional)
Front speakers
Power amplifier input
Rear output
Power amplifier (optional)
Rear speakers
Car antenna lead
Antenna extension cord (provided with the KTC-T100)
Hide-away unit
Tuner input
Changer input
Power input
Tuner KTC-T100 (optional)
Tuner output
Antenna input
Power connection cord
Ground lead (black) (−) To metal chassis of the car for ground
Battery
Engine key switch
ACC
Memory back-up power lead (yellow) (+)
Accessory power lead (red) (+)
Power antenna control lead (blue) (To fully-automatic power antenna)
Controller input
Changer extension cord
Controller extension cord
Changer
Changer output
Controller output
Controller

* If the installation location of the power amplifier is distant from the Hide-away unit, use the optionally available extension cable, CA-18F (1 m), CA-28F (2 m) or CA-48F (4 m).

CONNECTION

■ According to the mounting condition of the changer, hang the springs inside the covers on both sides as, shown in the figure below. (For shipping, the springs were hung for the horizontal mounting condition.)

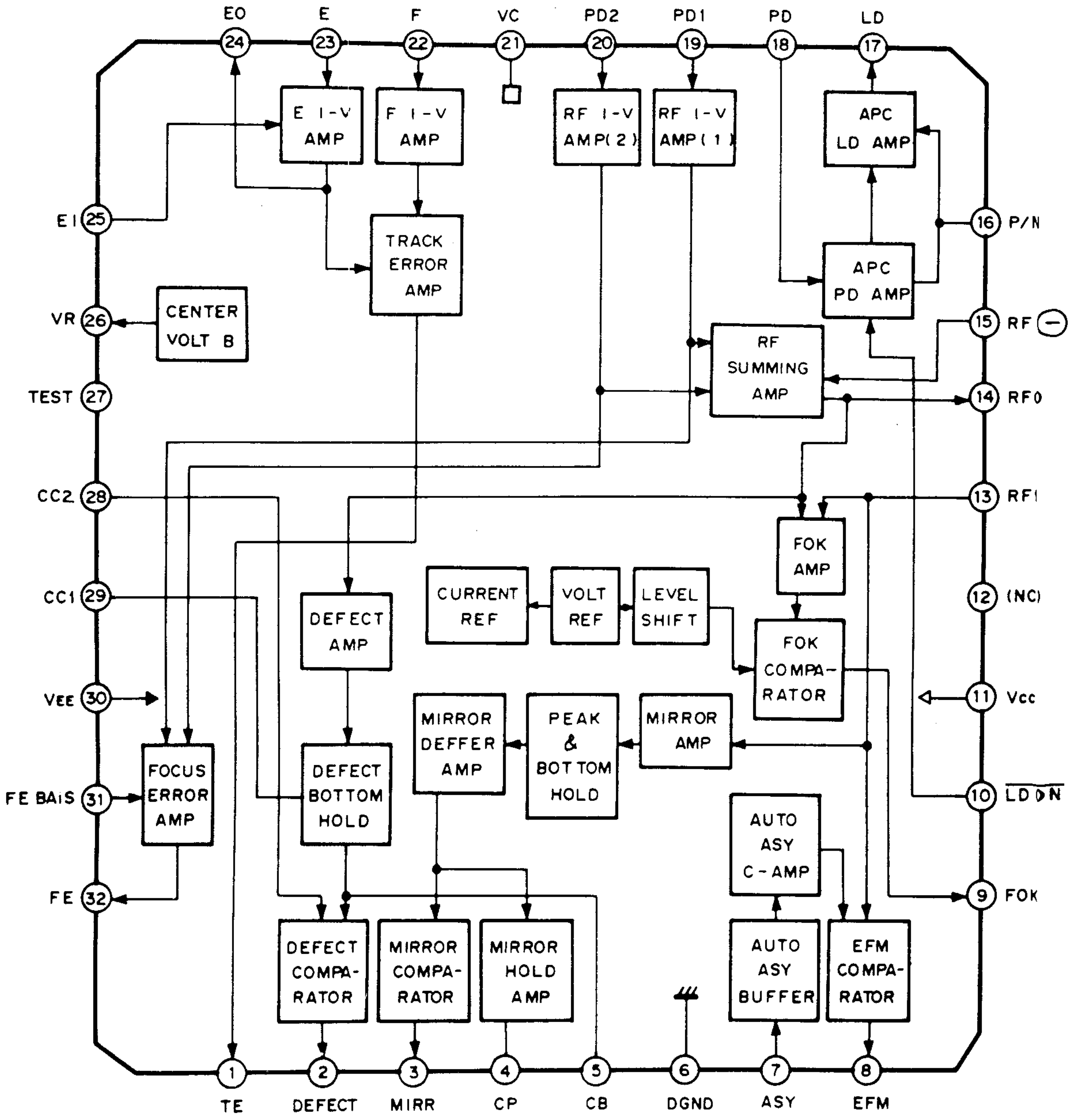


CIRCUIT DESCRIPTION

CXA1081Q RF amplifier

The CXA1081Q supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator


EO
E
F
VC
PD2
PD1
PD
LD
24
23
22
21
20
19
18
17
E I-V AMP
F I-V AMP
RF I-V AMP(2)
RF I-V AMP(1)
APC LD AMP
EI 25
16 P/N
TRACK ERROR AMP
APC PD AMP
VR 26
CENTER VOLT B
15 RF ⊖
RF SUMMING AMP
TEST 27
14 RFO
CC2 28
13 RFI
FOK AMP
CC1 29
12 (NC)
DEFECT AMP
CURRENT REF
VOLT REF
LEVEL SHIFT
FOK COMPA-RATOR
VEE 30
11 Vcc
MIRROR DEFFER AMP
PEAK & BOTTOM HOLD
MIRROR AMP
FOCUS ERROR AMP
DEFECT BOTTOM HOLD
FE BAIS 31
10 LD ON
AUTO ASY C-AMP
FE 32
9 FOK
DEFECT COMPA-RATOR
MIRROR COMPA-RATOR
MIRROR HOLD AMP
AUTO ASY BUFFER
EFM COMPA-RATOR
1
2
3
4
5
6
7
8
TE
DEFECT
MIRR
CP
CB
DGND
ASY
EFM

CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	TE	O	Tracking error amp output pin.
2	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10 kΩ load).
3	MIRR	O	Mirror compartor output pin. (DC voltage: connected to a 10 kΩ load).
4	CP	I	Mirror hold capacitro output pin. Mirror comparator non-invert input.
5	CB	I	Defect bottom hold capacitor connect pin.
6	DGND	—	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND (Vee) when using a single-voltage power supply.
7	ASY	I	Auto asymmetry control input pin..
8	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10 kΩ load).
9	FOK	O	FOK comparator output pin. (DC voltage: connected to a 10 kΩ load).
10	$\overline{\text{LD ON}}$	I	LD ON/OFF select pin. (DC voltage: when LD ON).
11	Vcc	—	Positive power supply.
13	RFI	I	Input pin of the C-coupled signal output from the RF summing amp.
14	RFO	O	Check point of eye pattern for the RF summing amp output pin.
15	RF ⊖	I	RF summing amp feedback input pin.
16	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
17	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
18	PD	I	APC PD amp input pin. (DC voltage: open)
19	PD1	I	RF I-V amp (1) invert input pin. Current input by connecting to PIN diode A+C.
20	PD2	I	RF I-V amp (2) invert input pin. Current input by connecting to PIN diode B+D.
21	VC	—	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
22	F	I	F I-V amp invert input pin. Current input by connecting to PIN diode F.
23	E	I	E I-V amp invert input pin. Current input by connecting to PIN diode E.
24	EO	O	E I-V amp output pin.
25	EI	I	E I-V amp feedback input pin. For E I-V amp gain adjustment.
26	VR	O	DC voltage ouput pin of (Vcc+Vee)/2.
27	TEST	—	Open
28	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
29	CC1	O	Defect bottom hold output pin.
30	Vee	—	Connected to the negative power supply when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
31	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
32	FE	O	Focus error amp output pin.

CIRCUIT DESCRIPTION

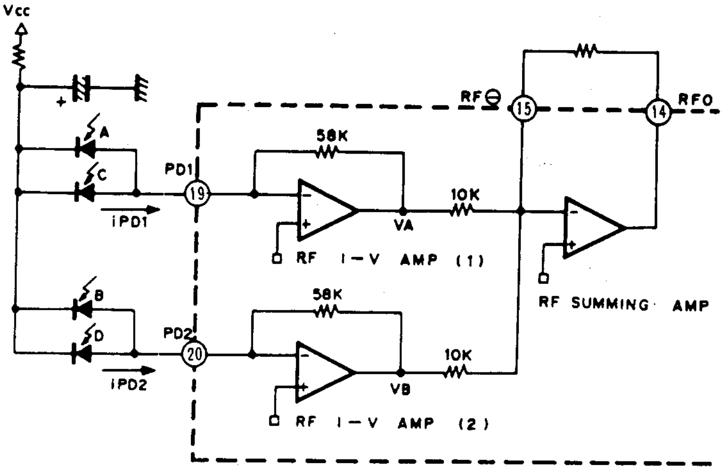
Explanation of function

- **RF amp**

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I–V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6k\Omega \times (i_{PD1} + i_{PD2})$$


Vcc
A
C
B
D
PD1
PD2
iPD1
iPD2
19
20
58K
58K
VA
VB
10K
10K
RF I–V AMP (1)
RF I–V AMP (2)
RF⊖
15
14
RFO
RF SUMMING AMP

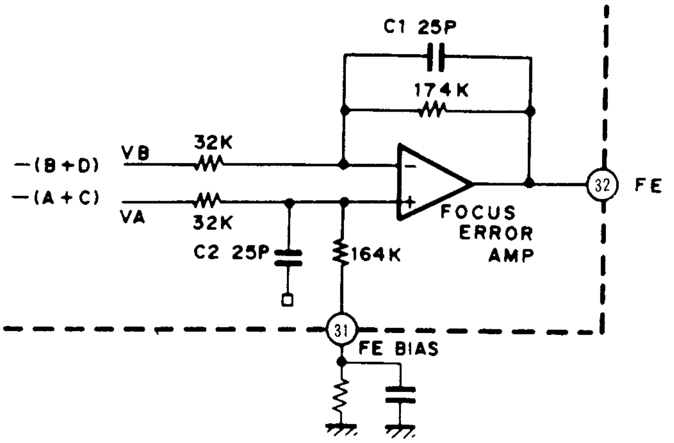
RF I–V amplifier

- **Focus error amp**

The difference between the RF I–V amp (1) output (VA) and the RF I–V amp (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4k\Omega$$


C1 25P
174K
–(B+D)
–(A+C)
VB
VA
32K
32K
C2 25P
164K
FOCUS ERROR AMP
32
FE
31
FE BIAS

CIRCUIT DESCRIPTION

- **Tracking error amp**

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I–V amp and F I–V amp respectively. That is:

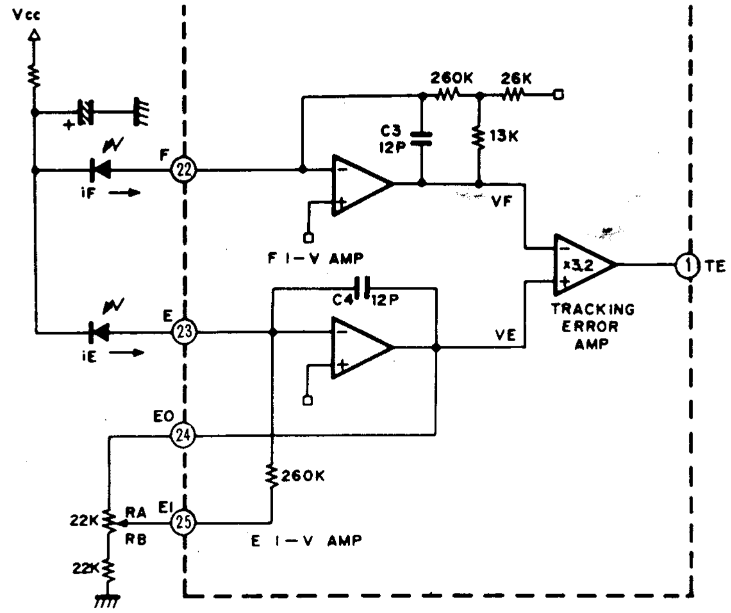
$$V_F = iF \times 403k\Omega$$

$$V_E = iE \times 260k\Omega \times R_A/(R_B + 22k) + (R_A + 260k)$$

The difference between the E I–V amp and the F I–V amp is calculated by the tracking error amp, and the photodiode (E–F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2$$

$$= (iE - iF) \times 1290k\Omega$$


Vcc
260K
26K
C3
12P
13K
F
22
iF
VF
F I–V AMP
x3.2
1
TE
C4
12P
TRACKING ERROR AMP
E
23
iE
VE
EO
24
260K
22K
RA
RB
EI
25
E I–V AMP
22K

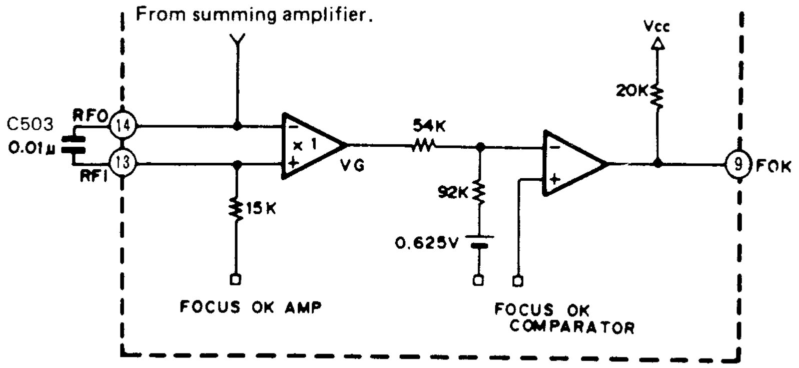
- **Focus OK circuit**

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RFI} - V_{RFO} \fallingdotseq -0.37V$.

C503 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C503 = 0.01µF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.


From summing amplifier.
Vcc
20K
C503
0.01µ
RFO
14
13
RFI
x 1
VG
54K
92K
0.625V
15K
9
FOK
FOCUS OK AMP
FOCUS OK COMPARATOR

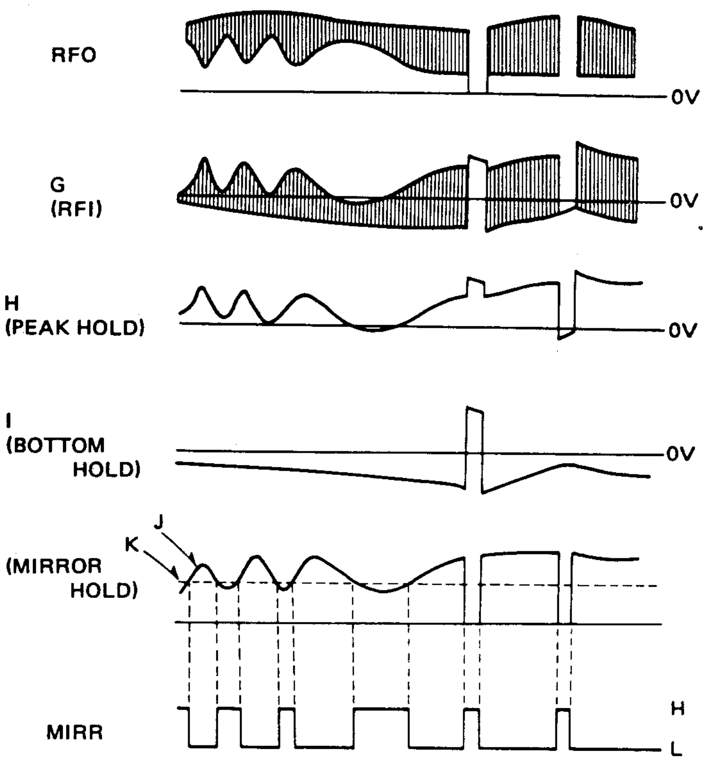
CIRCUIT DESCRIPTION

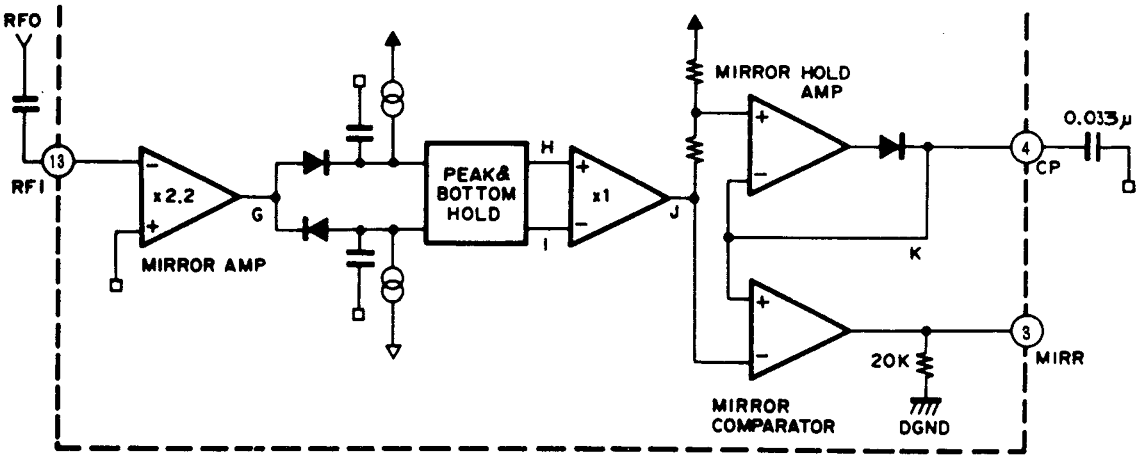
- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.




RFO
13
RFI
x2.2
MIRROR AMP
G
PEAK& BOTTOM HOLD
H
I
x1
J
MIRROR HOLD AMP
0.033μ
4
CP
K
3
MIRR
20K
DGND
MIRROR COMPARATOR

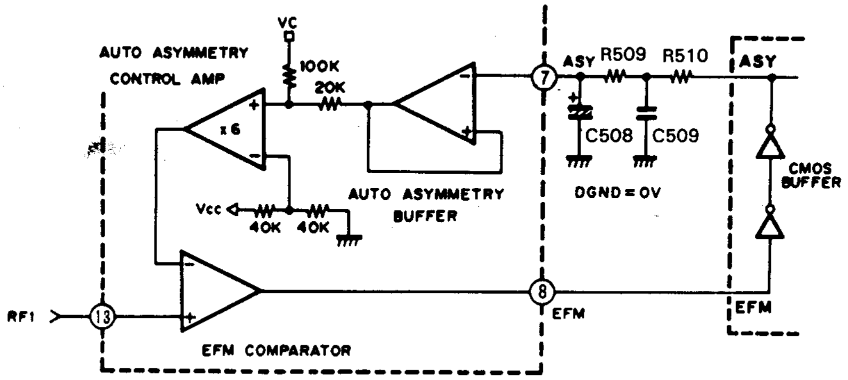
CIRCUIT DESCRIPTION

- **EFM comparator**

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

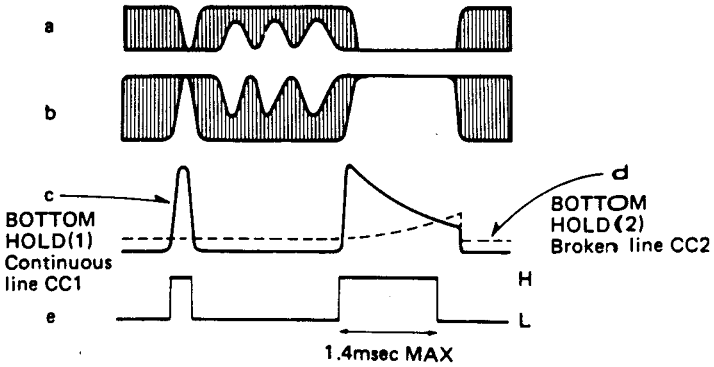
The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer.

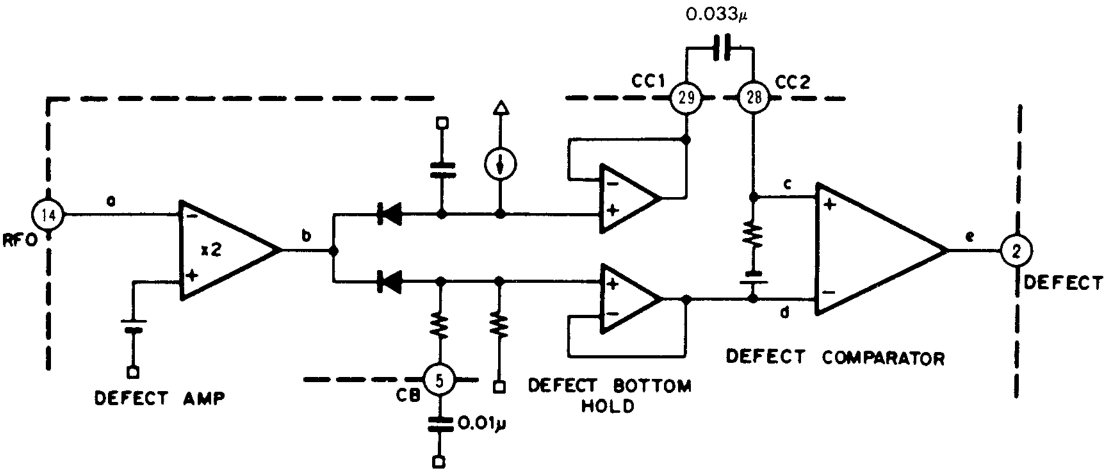
R509, R510, C508 and C509 constitute a LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.


VC
AUTO ASYMMETRY CONTROL AMP
100K
20K
x6
Vcc
40K
40K
AUTO ASYMMETRY BUFFER
7
ASY
R509
R510
C508
C509
DGND = 0V
ASY
CMOS BUFFER
8
EFM
EFM
RFI
13
EFM COMPARATOR

- **Defect circuit**

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generates the mirror defect detecting signals.




0.033μ
CC1
29
CC2
28
RFO
14
a
x2
b
c
e
2
DEFECT
d
DEFECT AMP
CB
5
0.01μ
DEFECT BOTTOM HOLD
DEFECT COMPARATOR

CIRCUIT DESCRIPTION

CXA1082AQ Servo signal processor for the CD

General

The CXA1082AQ is a bipolar IC developed for servo control in Compact Disc players.

Features

- Operates on a signal +5 V power supply as well as on a ±5 V dual-voltage power supply.
- Low power consumption (165 mW with ±5 V, 100 mW with +5 V).
- Same servo function as CX20108 (focusing, tracking, sled servo)
- Built-in auto sequencer.
- Built-in spindle servo LPF.
- Built-in loop filter and VCO for an EFM clock generating PLL.
- A minimum of external parts required.
- Sled overrun prevention circuit.
- Disc defect treatment circuit.
- Anti-shock circuit
- Linear motor feed for high-speed access.
- Shared use of a serial data bus with the CX23035 and CXD1135Q.
- The microprocessor and software both have upward compatibility with the CX20108.
- The pulse height of the focusing search, track jump, and sled kick can be set with externally connected resistors.

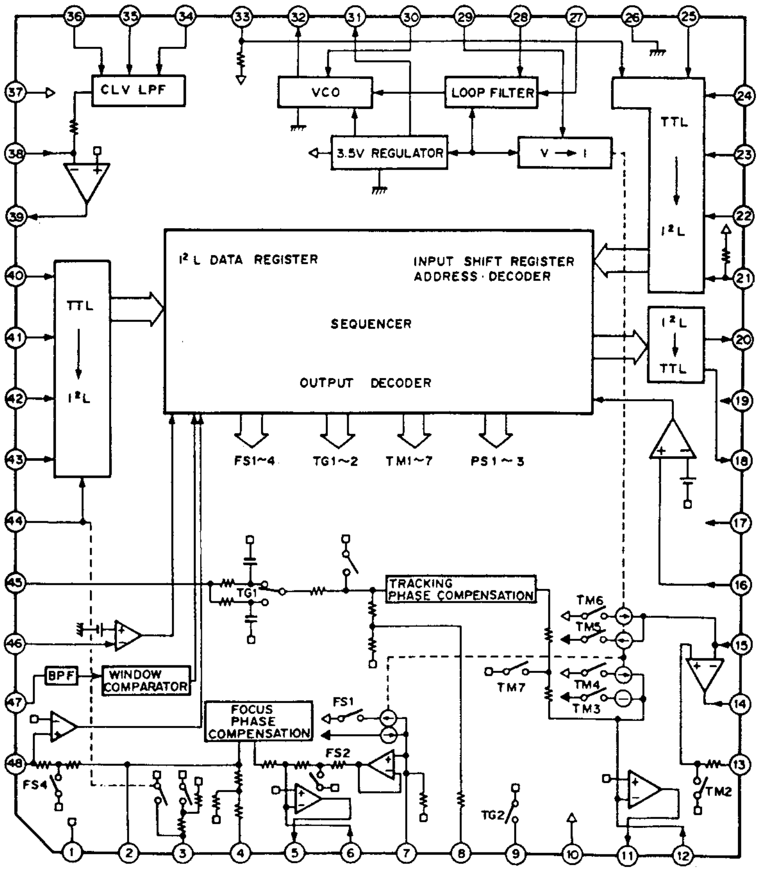
Functions

- Focusing servo control
- Tracking servo control
- Sled servo control
- Spindle servo
  Low Pass Filter, drive amplifier
- EFM clock generating PLL
  Loop filter: 8.64 MHz VCO
- Auto sequencer
  Incorporating a RAM

Structure

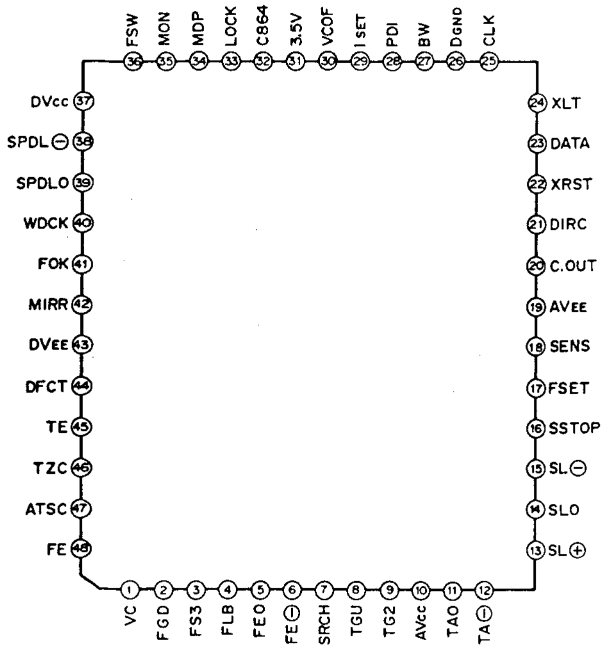
Bipolar silicon monolithic IC

Block diagram


CLV LPF
VCO
LOOP FILTER
3.5V REGULATOR
V → I
TTL
I²L
I²L DATA REGISTER
INPUT SHIFT REGISTER
ADDRESS · DECODER
SEQUENCER
OUTPUT DECODER
FS1~4
TG1~2
TM1~7
PS1~3
TRACKING PHASE COMPENSATION
TG1
TM6
TM5
TM7
TM4
TM3
BPF
WINDOW COMPARATOR
FOCUS PHASE COMPENSATION
FS1
FS2
FS4
TG2
TM2
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48

CIRCUIT DESCRIPTION

Pin configuration

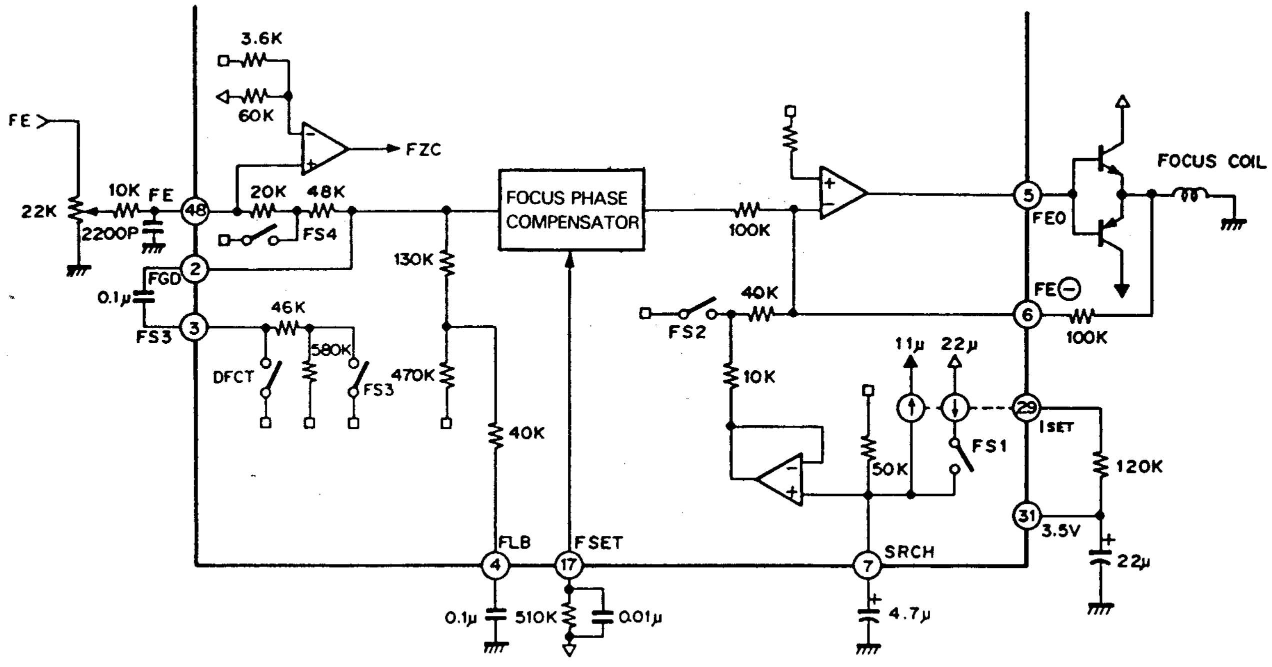

FSW 36
MON 35
MDP 34
LOCK 33
C864 32
3.5V 31
VCOF 30
I SET 29
PDI 28
BW 27
DGND 26
CLK 25
DVcc 37
SPDL⊖ 38
SPDLO 39
WDCK 40
FOK 41
MIRR 42
DVEE 43
DFCT 44
TE 45
TZC 46
ATSC 47
FE 48
24 XLT
23 DATA
22 XRST
21 DIRC
20 C.OUT
19 AVEE
18 SENS
17 FSET
16 SSTOP
15 SL⊖
14 SLO
13 SL⊕
1 VC
2 FGD
3 FS3
4 FLB
5 FEO
6 FE⊖
7 SRCH
8 TGU
9 TG2
10 AVcc
11 TAO
12 TA⊖

Terminal explanations

Terminal No.	Terminal name	Function
2	FGD	To lower the high frequency gain of the focus servo, insert a capacitor between this pin and pin 3.
3	FS3	The high frequency gain of the focus servo is selected by switching FS3 ON/OFF.
4	FLB	Time constant external connect pin, for boosting the focus servo low frequencies.
5	FEO	Power transistor drive op amplifier output pins.
11	TAO	
14	SLO	
39	SPDLO	
6	FE⊖	Focus amplifier inverted input pin.
7	SRCH	Time constant external connect pin, for creating the focus search waveform.
8	TGU	Time constant external connect pin, for selecting the tracking high frequency gain.
9	TG2	Time constant external connect pin, for selecting the tracking high frequency gain.
12	TA⊖	Tracking amplifier inverted input pin.
13	SL⊕	Sled amplifier non-inverted input pin.
15	SL⊖	Sled amplifier inverted input pin.
16	SSTOP	Limit switch ON/OFF detection signal input pin, for detecting the innermost edge of the disc.
17	FSET	Setting pin for the focus tracking phase peak value compensation, and fo of the CLV LPF.
18	SENS	Output pins for an interface with a microprocessor.
20	C.OUT	
21	DIRCT	Input pins for an interface with a microprocessor. A 47-kohm pull-up resistor is only incorporated in pins 21 and 33.
22	XRST	
23	DATA	
24	XLT	
25	CLK	
33	LOCK	
27	BW	Loop filter time constant external connect pin.
28	PDI	Input pin for the phase comparator output PDO of CXD23035/CXD1135.
29	ISET	Inputs a current which determines the level of the focus search, track jump, and sled kick.
30	VCOF	The self-advancing frequency of the VCO is almost proportional to the resistance between this pin and pin 31.
32	C864	8.64 MHz VCO output pin.
34	MDP	CXD23035/CXD1135 MDP pin connect pin.
35	MON	CXD23035/CXD1135 MON pin connect pin.
36	FSW	LPF time constant external connect pin, for the CLV servo error signal.
38	SPDL⊖	Spindle drive amplifier inverted input pin.
40	WDCK	Input pins for an interface with a microprocessor.
41	FOK	
42	MIRR	
44	DFCT	
45	TE	Tracking error signal input pin.
46	TZC	Tracking zero-cross comparator input pin.
47	ATSC	Window comparator input pin for ATSC detection.
48	FE	Focusing error signal input pin.

CIRCUIT DESCRIPTION

Focusing servo system


FE
22K
10K
FE
2200P
48
FGD
2
0.1μ
FS3
3
3.6K
60K
FZC
20K
48K
FS4
130K
46K
580K
DFCT
FS3
470K
40K
FOCUS PHASE COMPENSATOR
100K
40K
FS2
10K
11μ
22μ
50K
FS1
5
FEO
FE⊖
6
100K
29
ISET
120K
31
3.5V
22μ
FOCUS COIL
FLB
4
FSET
17
7
SRCH
0.1μ
510K
0.01μ
4.7μ

This block diagram is of the focusing servo system.

When FS3 is ON, the capacitor connected between pins 2 and 3 and the internal resistance determines the low-frequency time constant which can attenuate the high-frequency gain.

The capacitor between pin 4 and GND determines the time constant for boosting the low frequencies in normal playback.

The peak frequency of the focusing phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

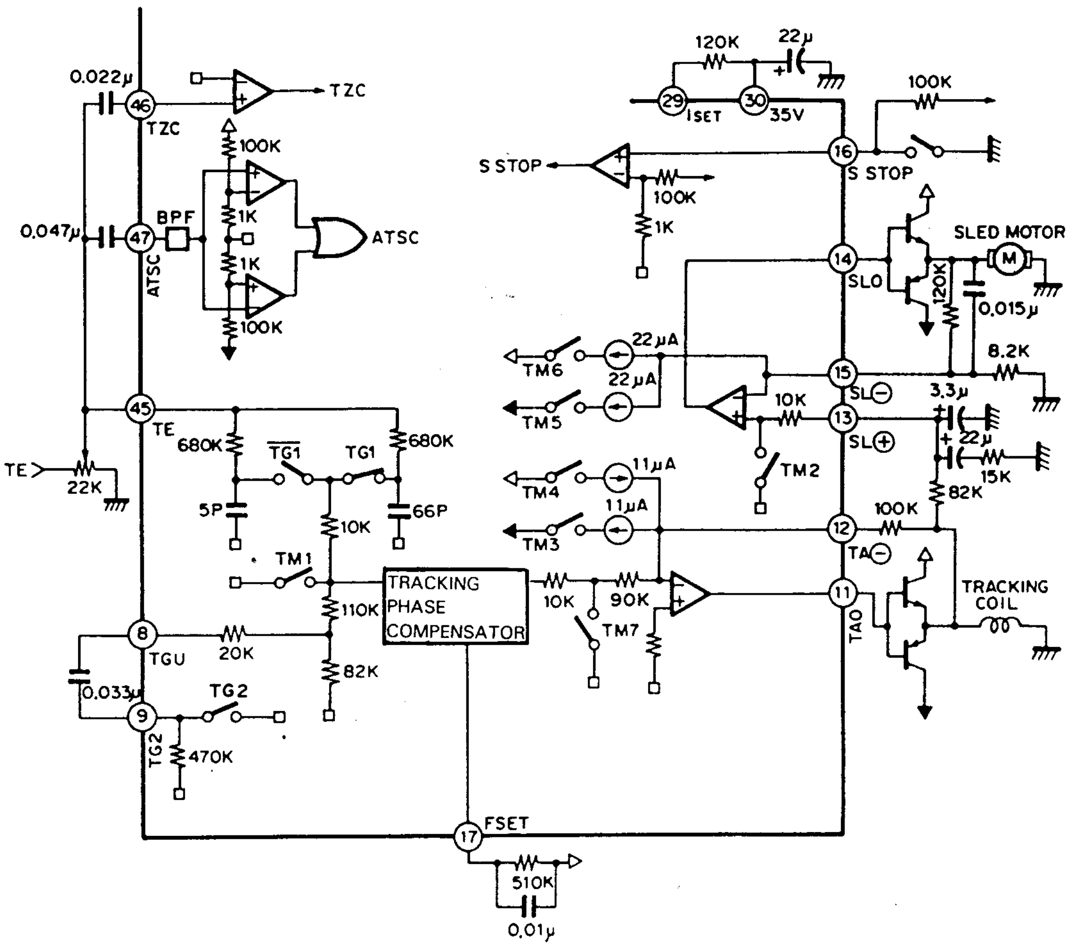
The focus search level is about ±1.1 Vp-p with these constants. The level is inversely proportional to the value of the resistance connected between pins 29 and 30. Note that the track jump and sled kick levels are also varied by changing this resistance.

The level has been set to 5.7% of the difference between Vcc, the inverted input reference voltage of the FZC comparator, and VC (pin 1); i.e. (Vcc − VC) × 5.7%.

- Varying the value of resistance connected to pin 17 also varies the phase compensation peak values of focusing/tracking/sled servos and fc of the CVL LPF. At the same time, the op amplifier's dynamic range and offset voltage are also varied.

CIRCUIT DESCRIPTION

Tracking and sled servo system


0.022μ
46
TZC
TZC
100K
0.047μ
47
BPF
1K
1K
ATSC
ATSC
100K
45
TE
TE
22K
680K
TG1
TG1
680K
5P
66P
10K
TM1
TRACKING PHASE COMPENSATOR
110K
8
TGU
20K
0.033μ
82K
TG2
9
TG2
470K
FSET
17
510K
0.01μ
120K
22μ
29
ISET
30
35V
100K
S STOP
16
S STOP
100K
1K
14
SLO
SLED MOTOR
M
120K
0.015μ
8.2K
22μA
TM6
22μA
TM5
15
SL⊖
10K
13
SL⊕
TM2
3.3μ
22μ
15K
82K
11μA
TM4
11μA
TM3
12
100K
TA⊖
10K
90K
TM7
11
TAO
TRACKING COIL

This block diagram is of the tracking and sled servo system. The capacitor connected between pins 8 and 9 determines the time constant for attenuating the high-frequency gain. The peak frequency for the tracking phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

A FWD or REV tracking jump is performed by switching TM3 or TM4 ON. At this time, the peak voltage applied to the tracking coil depends on the current at TM3 or TM4 and the feedback resistance through pin 12, as shown by the following equation:

Track jump peak voltage = TM3 (TM4) current × Feedback resistance

A FWD or REV sled kick is performed by switching TM5 or TM6 ON. At this time, the peak voltage applied to the sled motor depends on the current at TM5 or TM6 and the feedback resistance through pin 15, as shown by the following equation.

Sled jump peak voltage = TM5 (TM6) current × Feedback resistance

The currents at these switches are determined by the resistance connected between pins 29 and 31. When the value is 120 k-ohms, the currents are:

±11 μA at TM3 and TM4, and

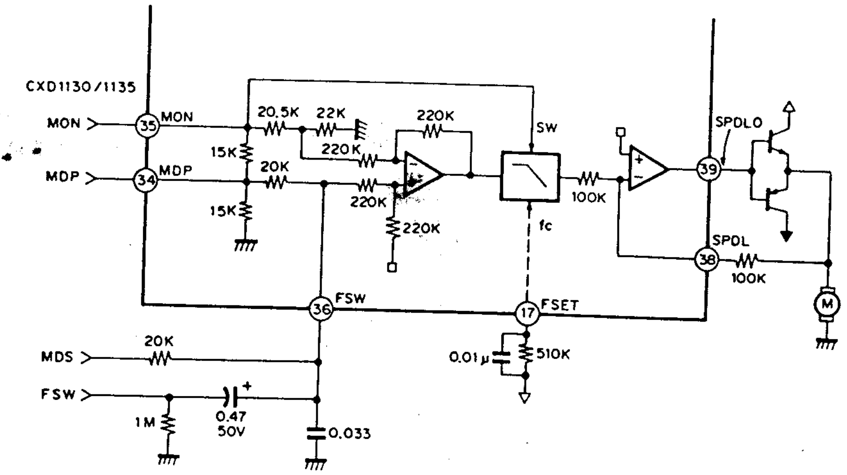
±22 μA at TM5 and TM6.

The currents are inversely proportional to the resistance, and the variable range is from about 5 to 40 μA with TM3.

S STOP is the signal used to detect the ON/OFF of the limit switch for detecting the innermost position for the linear motor.

CIRCUIT DESCRIPTION

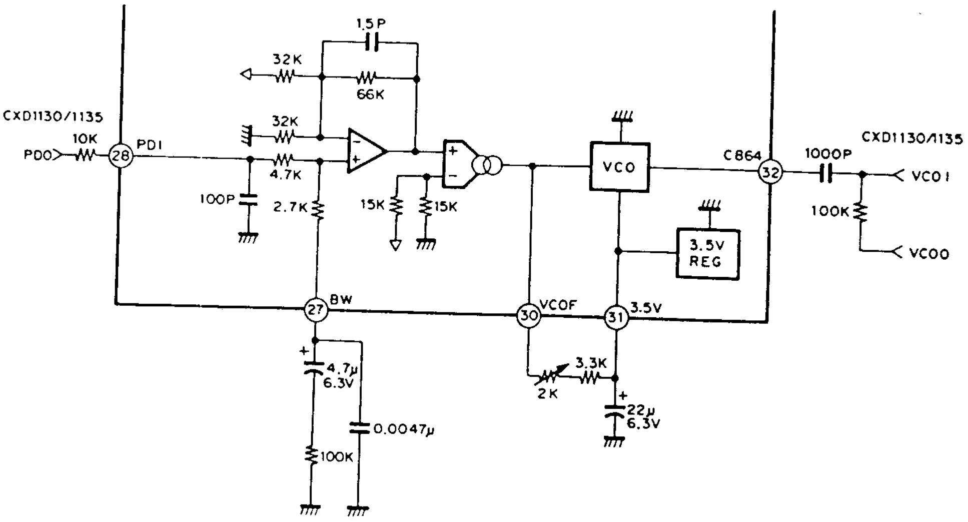
Spindle servo and LPF circuitry


CXD1130/1135
MON
MON
35
MDP
MDP
34
20.5K
22K
220K
220K
15K
20K
15K
220K
220K
SW
100K
fc
SPDLO
39
SPDL
38
100K
M
FSW
36
FSET
17
MDS
20K
FSW
1M
0.47
50V
0.033
0.01μ
510K

The carrier component in the CLV servo error signals MDS and MDP are eliminated by a two-stage LPF, which consists of a 200 Hz LPF formed by a 0.033 μF capacitor and a 20 k-ohms resistor connected to pin 36 and an internal LPF (fc up to 200 Hz when 510 k-ohms is connected to pin 17).

In the CLV-S mode, FSW becomes L, and fc of the LPF at pin 36 drops to enhance the filtering effect. The resistor connected to pin 17 need not be stabilized but only connected to Vcc, because its fc will not be varied by supply voltage variation.

VCO loop filter and 8.64 MHz VCO circuitry


CXD1130/1135
10K
PDO
28
PDI
1.5P
32K
66K
32K
4.7K
100P
2.7K
15K
15K
VCO
C864
32
1000P
CXD1130/1135
VCOI
100K
VCOO
3.5V
REG
BW
27
VCOF
30
31
3.5V
4.7μ
6.3V
0.0047μ
100K
3.3K
2K
22μ
6.3V

The phase comparator output, PDO, is input via pin 28, sent through the loop filter to eliminate the PWM carrier component, then V-I converted, and added with the self-advancing frequency set current from pin 30 for use in controlling the VCO frequency. The VCO's self-advancing frequency is almost proportional to the resistance connected between pins 30 and 31. The value of this resistance is set so that the PLL capture range center is 4.3218 MHz at CXD1135/1130 pin 70. The external circuit connected to pin 27 BW is used to maximize the capture range during accessing, so that access is possible even when the self-advancing frequency deviates due to the VCO's temperature characteristic, etc.

CIRCUIT DESCRIPTION

CXD1130Q Digital signal processing LSI for the CD

General

The CXD1130Q is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter

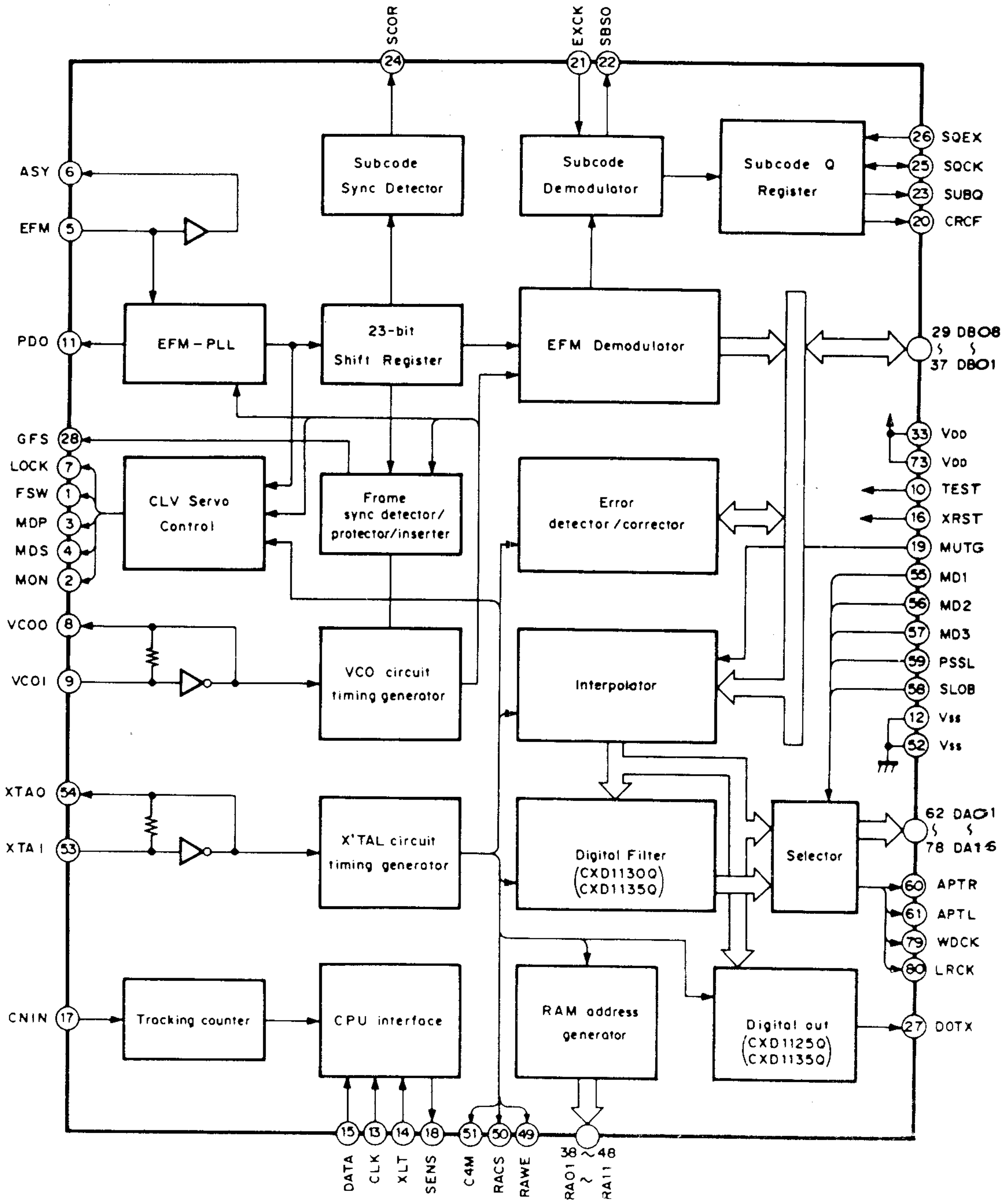
Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

Block diagram


SCOR
EXCK
SBSO
24
21
22
Subcode Sync Detector
Subcode Demodulator
Subcode Q Register
26 SQEX
25 SQCK
23 SUBQ
20 CRCF
ASY 6
EFM 5
PDO 11
EFM-PLL
23-bit Shift Register
EFM Demodulator
29 DB08 ~ 37 DB01
GFS 28
LOCK 7
FSW 1
MDP 3
MDS 4
MON 2
CLV Servo Control
Frame sync detector/ protector/inserter
Error detector/corrector
33 VDD
73 VDD
10 TEST
16 XRST
19 MUTG
55 MD1
56 MD2
57 MD3
59 PSSL
58 SLOB
12 Vss
52 Vss
VCOO 8
VCOI 9
VCO circuit timing generator
Interpolator
XTAO 54
XTAI 53
X'TAL circuit timing generator
Digital Filter (CXD1130Q CXD1135Q)
Selector
62 DA01 ~ 78 DA16
60 APTR
61 APTL
79 WDCK
80 LRCK
CNIN 17
Tracking counter
CPU interface
RAM address generator
Digital out (CXD1125Q CXD1135Q)
27 DOTX
15 DATA
13 CLK
14 XLT
18 SENS
51 C4M
50 RACS
49 RAWE
38 ~ 48
RA01 ~ RA11

CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L"
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\mathrm{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f= 4.2336 MHz.
52	Vss	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL="H", C1F1 output when PSSL="L".
63	DA02	O	DA02 output when PSSL="H", C1F2 output when PSSL="L".
64	DA03	O	DA03 output when PSSL="H", C2F1 output when PSSL="L".
65	DA04	O	DA04 output when PSSL="H", C2F2 output when PSSL="L".
66	DA05	O	DA05 output when PSSL="H", C2FL output when PSSL="L".
67	DA06	O	DA06 output when PSSL="H", C2PO output when PSSL="L".
68	DA07	O	DA07 output when PSSL="H", RFCK output when PSSL="L".
69	DA08	O	DA08 output when PSSL="H", WFCK output when PSSL="L".
70	DA09	O	DA09 output when PSSL="H", $\overline{\text{PLCK}}$ output when PSSL="L".
71	DA10	O	DA10 output when PSSL="H", UGFS output when PSSL="L".
72	DA11	O	DA11 output when PSSL="H", GTOP output when PSSL="L".
73	VDD	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL="H", RAOV output when PSSL="L".
75	DA13	O	DA13 output when PSSL="H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL="H", $\overline{\text{C210}}$ output when PSSL="L".
77	DA15	O	DA15 output when PSSL="H", C210 output when PSSL="L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL="H", DATA output when PSSL="L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF.

Notes:

C1F1 :
C1F2 : Error correction status monitor output for C1 decode.
C2F1 :
C2F2 : Error correction status monitor output for C2 decode.
C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.
C2PO : C2 pointer signal. Synchronized to the audio data output.
RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.
WFCK : Write frame clock output. 7.35 MHz when locked to the crystal line.
$\overline{\text{PLCK}}$: VCO/2 output. f=4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.
GTOP : Frame sync protect status display output.
RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.
C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.
$\overline{\text{C210}}$: C210 invert output.
C210 : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.
DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

Explanation of functions

1. CPU interface

(1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 1 to three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 1, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

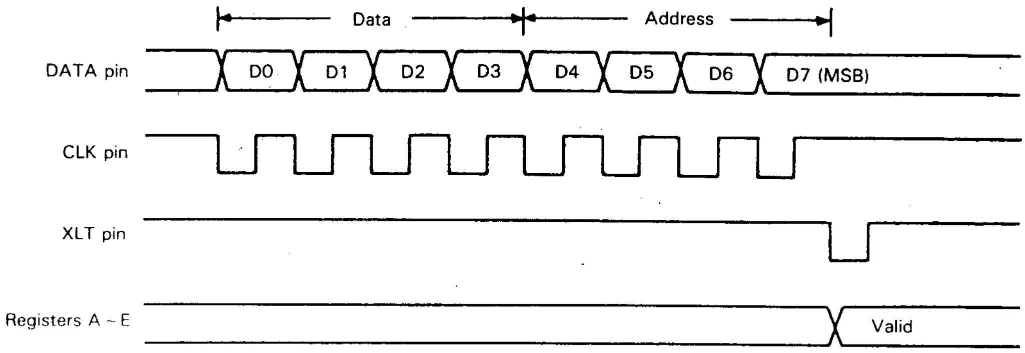


Fig. 1 Timing chart for data input

(2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 29)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 35)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**10. Countermeasures to defects**". (Page 42)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 40)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB.

D1 : WSEL
D2 : GSEL
D3 : GSEM — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 31)

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case.

CIRCUIT DESCRIPTION

Register E — CLV mode

It is as shown in Table 1.

The details of each mode will be described in "**6. CLV servo control**". (Page 37)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data				SENS pin
			D3	D2	D1	D0	
9[1]	New function control	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A[2]	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D[3]	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E[4]	CLV mode	1110	CLV mode				$\overline{\text{PW} \geq 64}$

[1] Register 9

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

[2] Register A

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

[3] Register D

DIV	D3	0	RFCK/4, WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8, WFCK/8	
T_B	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
T_P	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12 dB	Gain at MDP pin in CLV-S, CLV-H mode
		1	0 dB	

[4] Register E

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 1 List of registers

(3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal ($\overline{\text{COMPLETE}}$) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal ($\overline{\text{COUNT}}$) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 2.

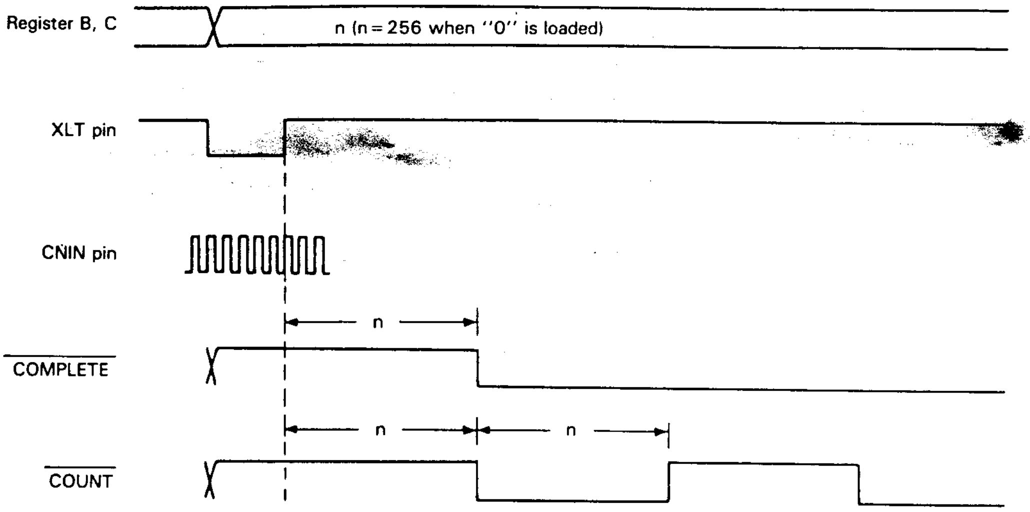


Fig. 2 Tracking counter timing chart

(4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) $\overline{\text{COMPLETE}}$: Address (see note) is "B"; Shown in Fig. 2.

(2) $\overline{\text{COUNT}}$: Address (see note) is "C"; Shown in Fig. 2.

(3) $\overline{\text{PW} \geq 64}$: Address (see note) is "E"; This signal is of LOW level when the pulse width after bottomhold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 1.

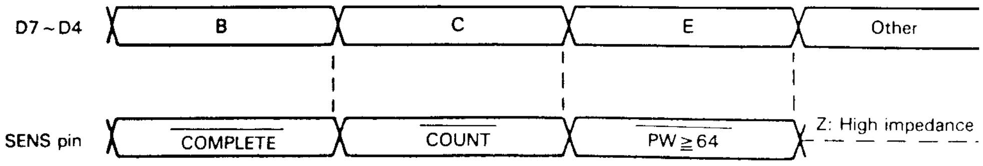


Fig. 3 Timing chart of SENS pin

CIRCUIT DESCRIPTION

(5) Sub code output

Sub codes P ~ W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0 + S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a. When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

b. When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated as shown in Fig. 7, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

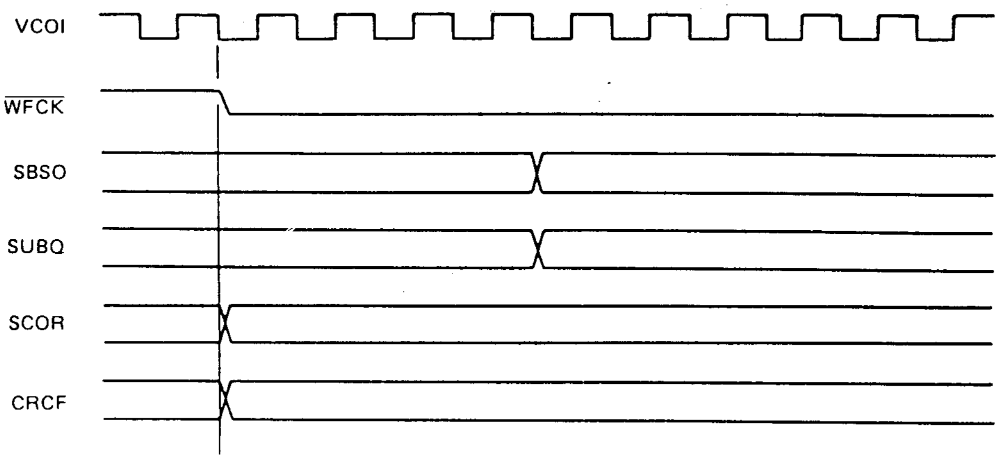
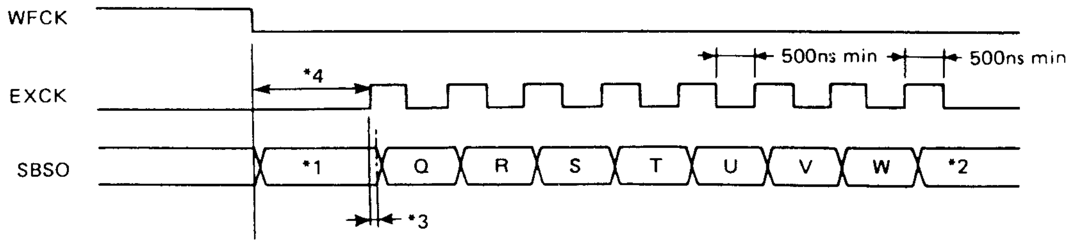


Fig. 4

(b) Timing of SBSO, EXCK



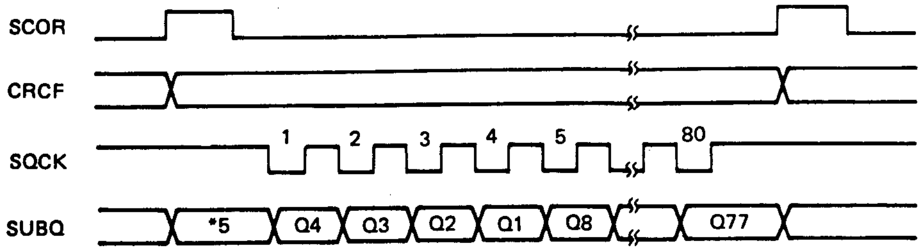
*1: Sub code P is output when SCOR is 0.
S0 + S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T ~ 6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T = 8.6436 MHz.

Fig. 5 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

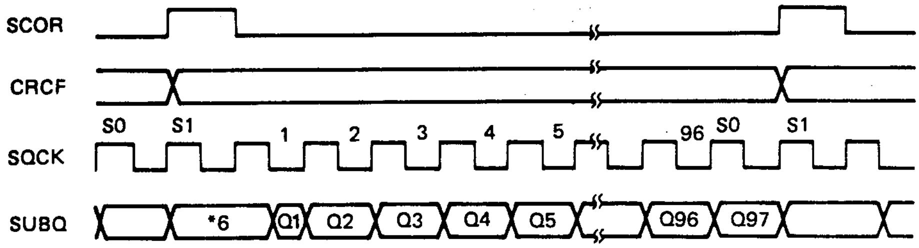
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5:CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6:CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 6 Timing chart of sub code outputs

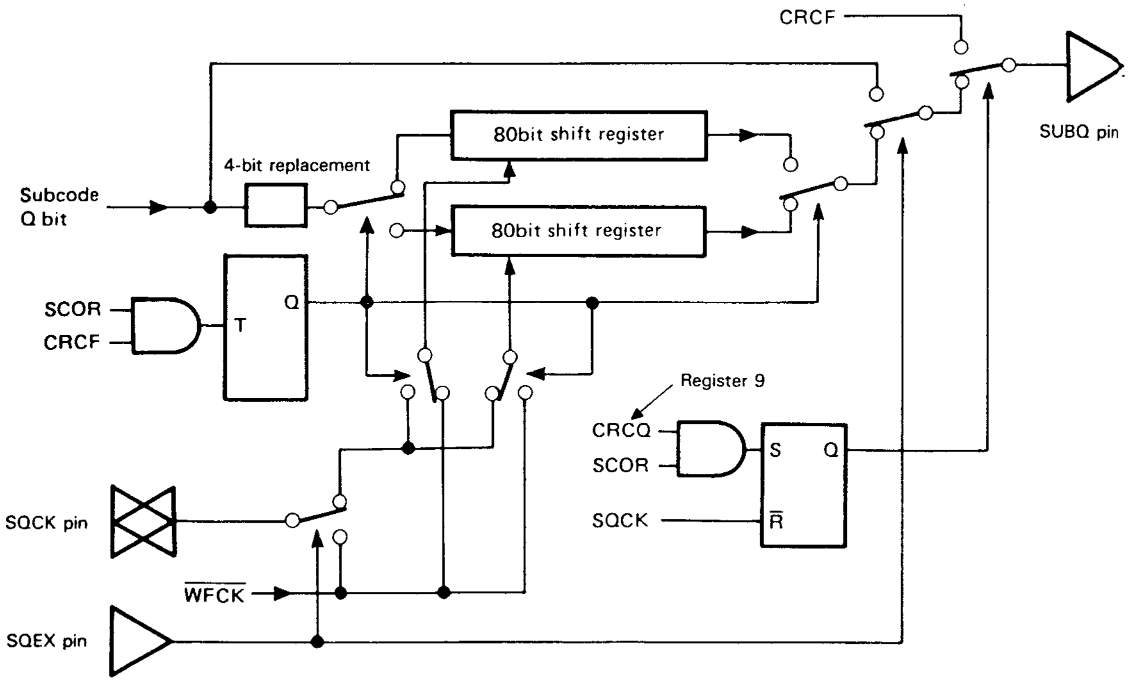

CRCF
SUBQ pin
80bit shift register
4-bit replacement
Subcode Q bit
80bit shift register
SCOR
CRCF
T
Q
Register 9
CRCQ
SCOR
SQCK
S
Q
$\overline{R}$
SQCK pin
$\overline{WFCK}$
SQEX pin

Fig. 7

CIRCUIT DESCRIPTION

2. EFM demodulation

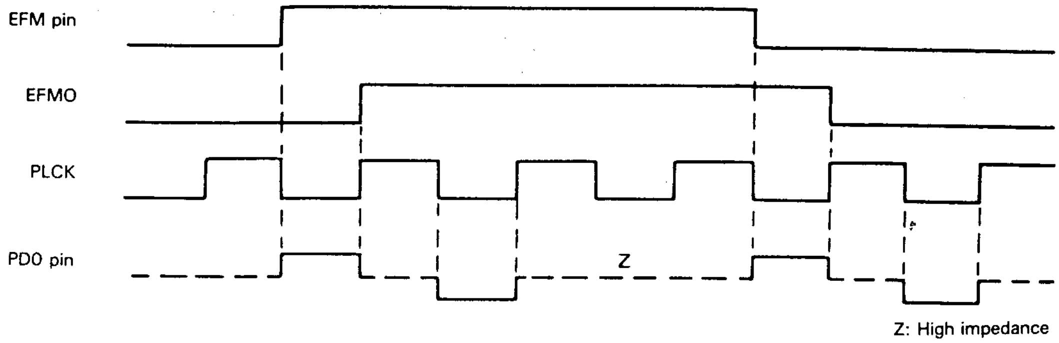
(1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.

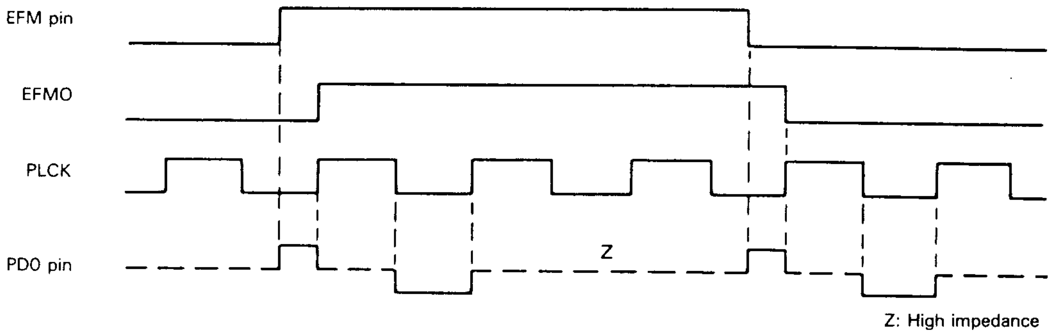
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 8.

(a) When EFM signal and VCO are synchronized


EFM pin
EFMO
PLCK
PDO pin
Z
Z: High impedance

(b) When VCO is higher than EFM signal


EFM pin
EFMO
PLCK
PDO pin
Z
Z: High impedance

(c) When VCO is less than EFM signal

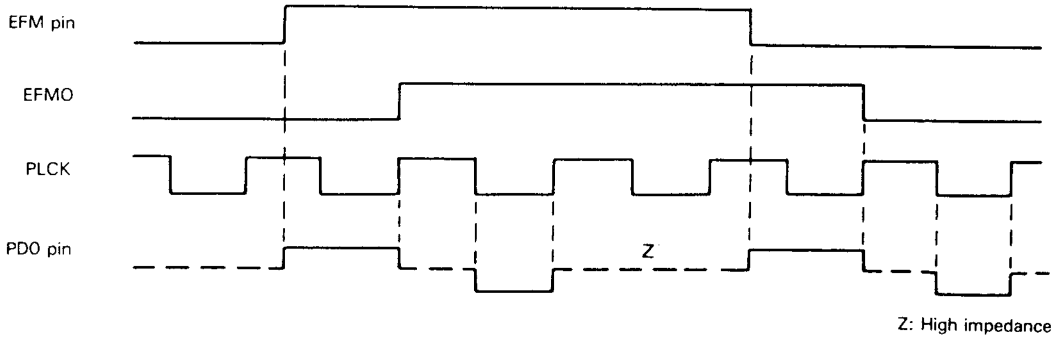

EFM pin
EFMO
PLCK
PDO pin
Z
Z: High impedance

Fig. 8 Timing charts of EFM-PLL circuit

(2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.

If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 = 7.35 kHz)

A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ). Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

(3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8-bit data through 14 →8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

3. Sub code demodulation

(1) Sub code demodulation

Synchronizing signals S0 and S1 of 14-bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0+S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).

Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.

The details of this timing will be shown in **"1. CPU interface"**. (Page 26)

(2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.

It goes "L" when an error is detected. If the CRCQflag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**.

CIRCUIT DESCRIPTION

4. RAM interface (generation of external RAM address)

(1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.

This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

(2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.

This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

(3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.

In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.

The requests from the error correction unit are of the lowest priority among requests of three types.

After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal.

This block generates type address of the requested data, and controls R/W of the RAM at the same time.

(4) Address generation

The data after EFM demodulation is data subjected to interleave processing.

This interleave processing is subjected to data lag by the unit of a frame.

Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer.

The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

(5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.

In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

(6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.

As a result, there is no case where data without error correction is output to the D/A.

The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

5. Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.

(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.

(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.

(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.

(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16-bit).

(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.

(7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows.

A data request is made from the correction block to the RAM interface block.

The RAM interface block accepts the request with the operating situation of the entire system observed. The address of the requested data is generated to the external RAM.

Read/Write of the correction block and RAM data are enabled.

(9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to "L" when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

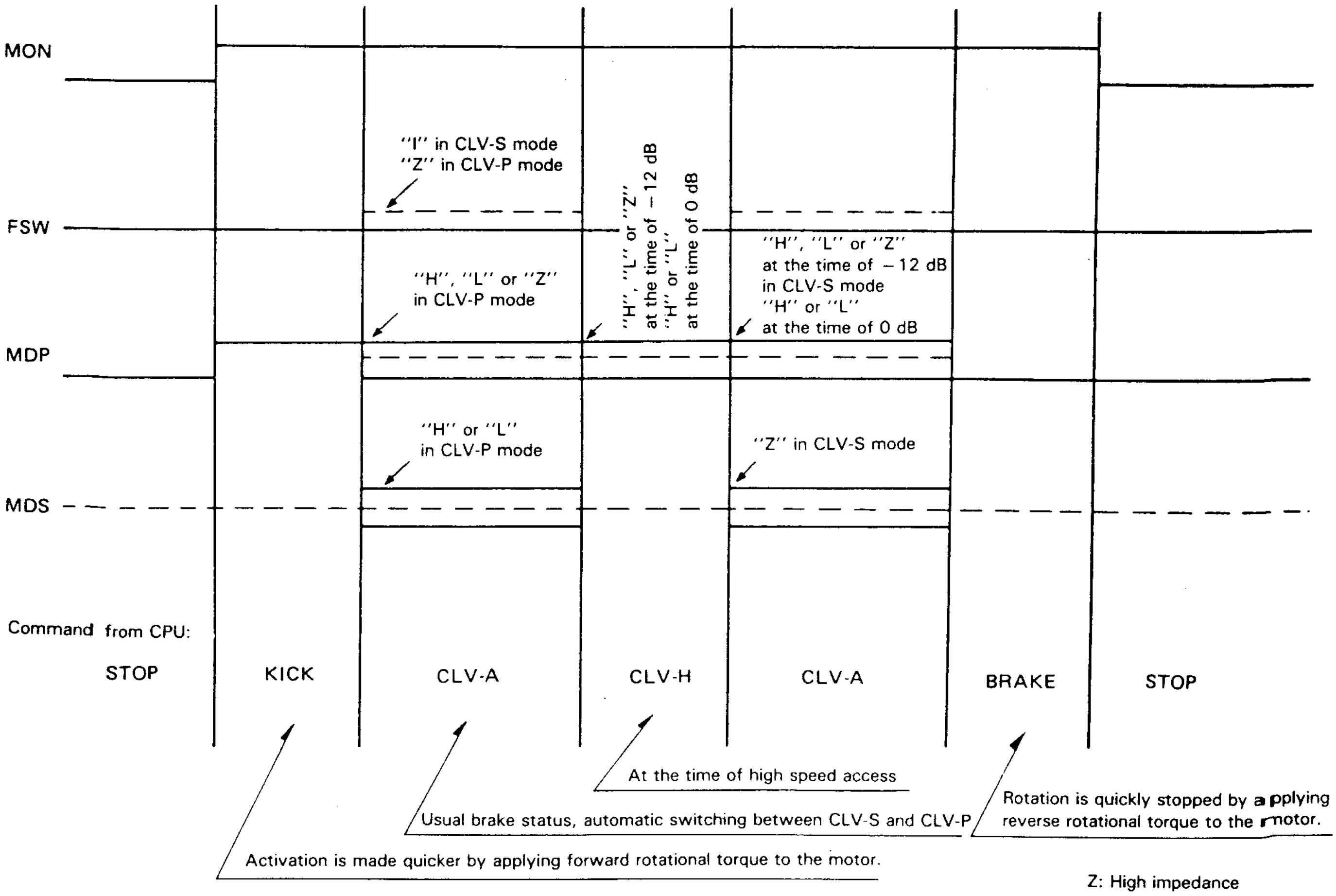
6. CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) STOP: Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

(2) KICK: Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

(3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".


MON
FSW
MDP
MDS
"I" in CLV-S mode
"Z" in CLV-P mode
"H", "L" or "Z"
in CLV-P mode
"H", "L" or "Z"
at the time of −12 dB
"H" or "L"
at the time of 0 dB
"H", "L" or "Z"
at the time of −12 dB
in CLV-S mode
"H" or "L"
at the time of 0 dB
"H" or "L"
in CLV-P mode
"Z" in CLV-S mode
Command from CPU:
STOP
KICK
CLV-A
CLV-H
CLV-A
BRAKE
STOP

At the time of high speed access

Usual brake status, automatic switching between CLV-S and CLV-P

Rotation is quickly stopped by applying reverse rotational torque to the motor.

Activation is made quicker by applying forward rotational torque to the motor.

Z: High impedance

Fig. 9 Typical control of spindle motor

(4) CLV-S: Register E = 1110'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.

When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.

"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B

Rough servo mode used at the time of high-speed access.

Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.

Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8.4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

Pwmdx: Pulse width after bottom hold
TB: Bottom hold period, i.e. RFCK/16 or RFCK/32
Z: High impedance

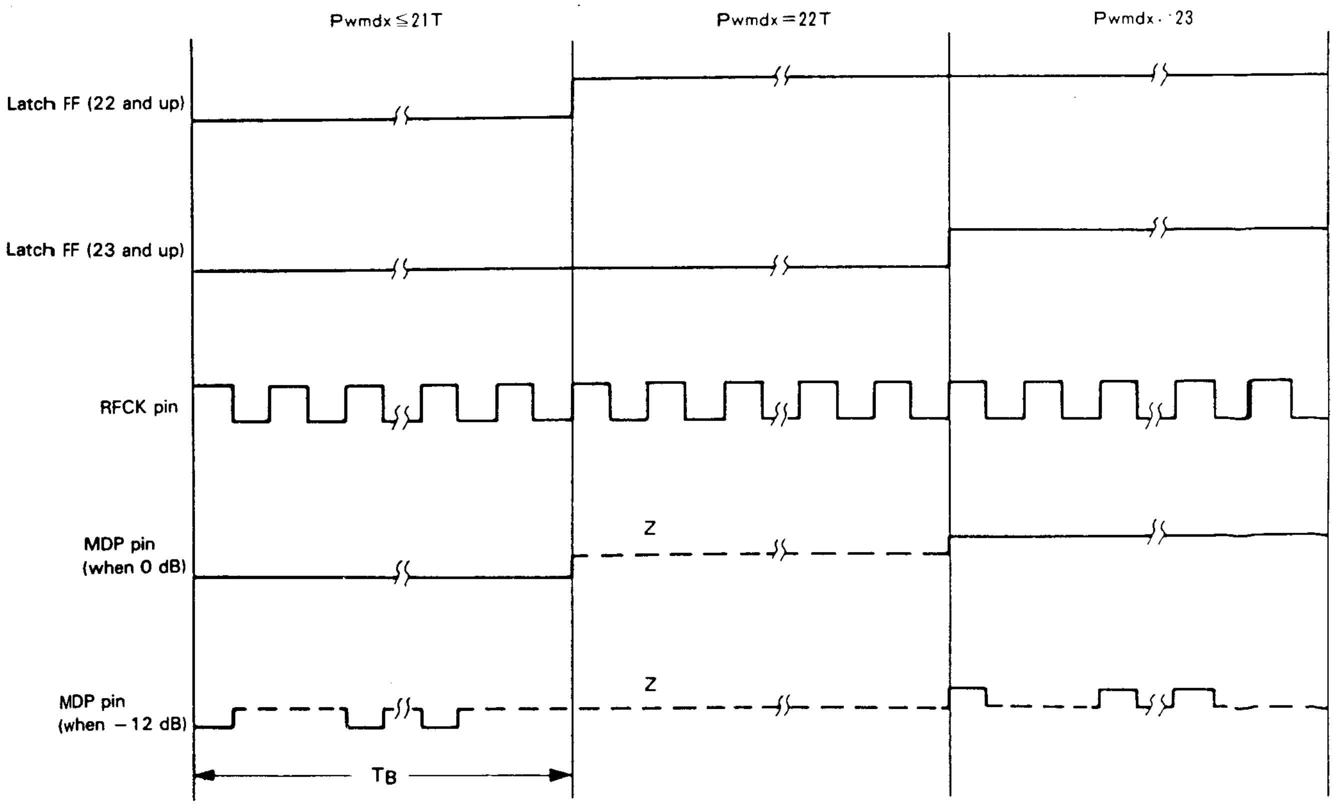


Fig. 10 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

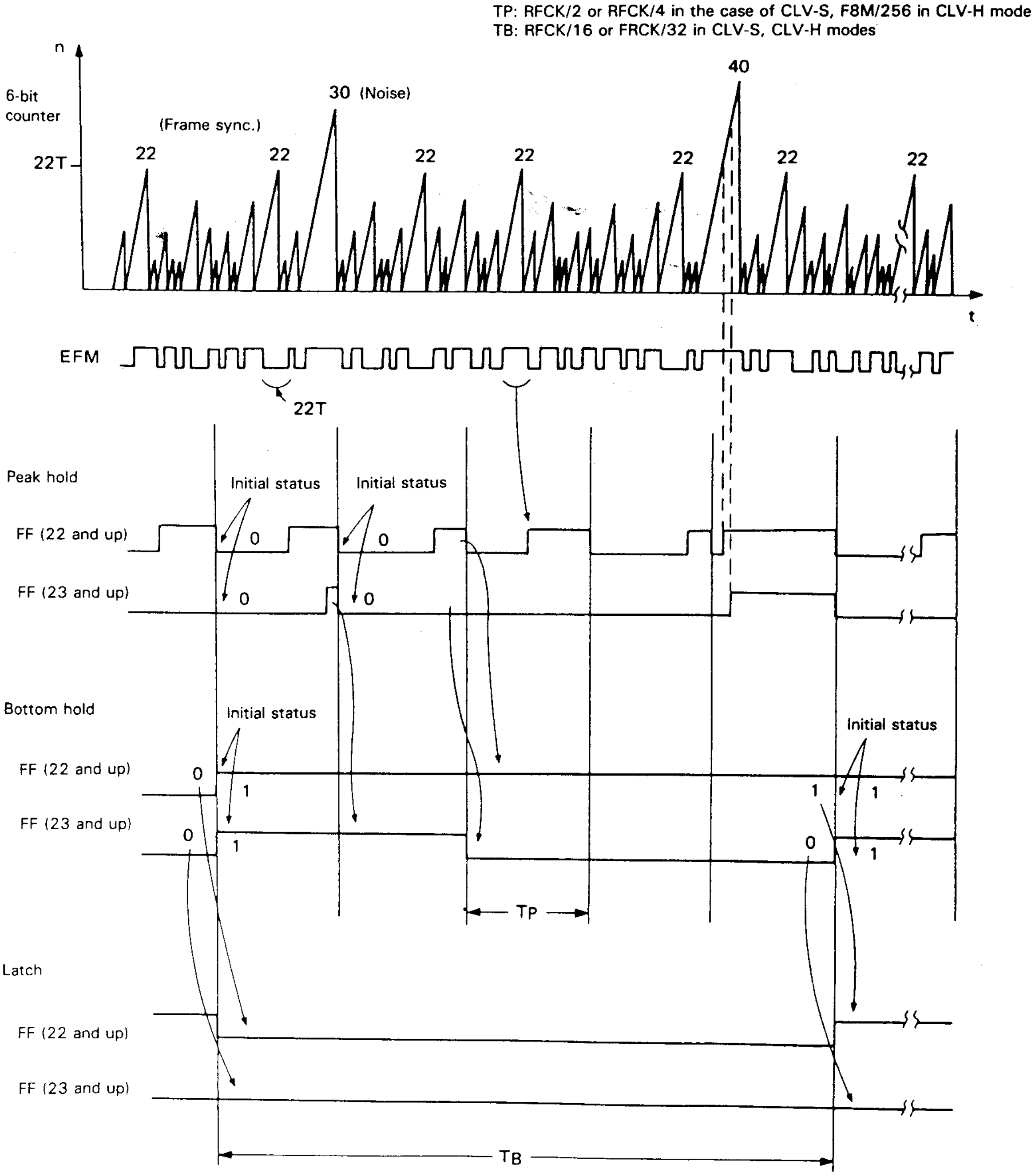

TP: RFCK/2 or RFCK/4 in the case of CLV-S, F8M/256 in CLV-H mode
TB: RFCK/16 or FRCK/32 in CLV-S, CLV-H modes
n
6-bit counter
22T
(Frame sync.)
22
22
30 (Noise)
22
22
22
40
22
22
t
EFM
22T
Peak hold
FF (22 and up)
FF (23 and up)
Initial status
Initial status
0
0
0
0
Bottom hold
Initial status
Initial status
FF (22 and up)
FF (23 and up)
0
1
0
1
1
1
0
1
TP
Latch
FF (22 and up)
FF (23 and up)
TB

Fig. 11 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B
PLL servo mode.

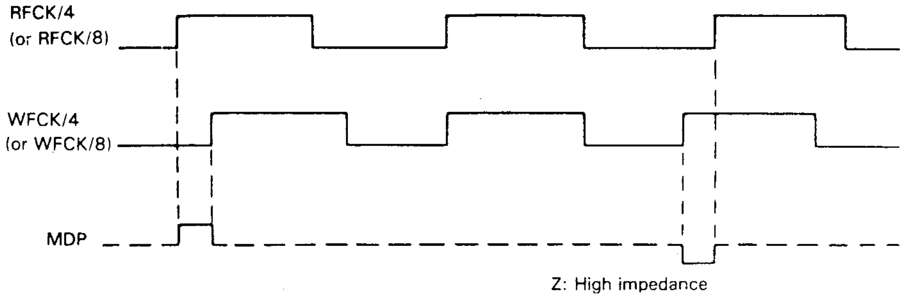
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.

Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (thw-279T) x 32, and then goes "L" until the next trailing edge of WFCK.

MDS = "H" when thw ≧ 279T,
MDS = "L" when thw ≦ 279T.

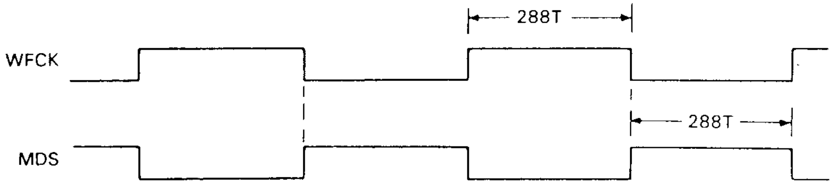
The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ thw ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

MDP pin

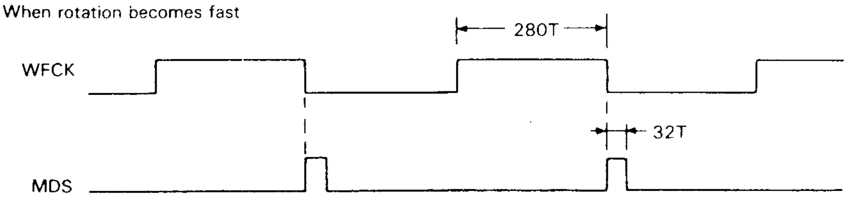


5) MDS pin (The period of 4.2336 MHz is expressed as "T".)

(1) When rotating at specified velocity



(2) When rotation becomes fast



(3) When rotation becomes slow

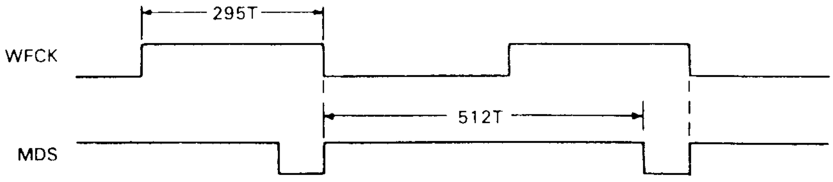


Fig. 12 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E=0110'B

The mode used for normal play status.

The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode.

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **"1. CPU interface"**. (Page 26)

Note:

When PSSL="L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E=0101'B

New auto servo mode added to the CX23035.

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

7. Interpolation and mute, attenuate

(1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.

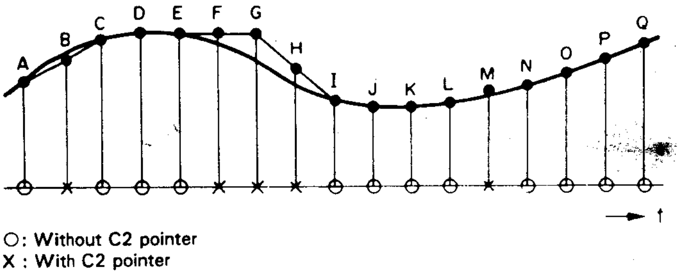


Fig. 13

Mean value interpolation

$$B = \frac{1}{2}(A + C)$$

$$H = \frac{1}{2}(E + I) \quad \text{: When pointers are continuous}$$

$$M = \frac{1}{2}(L + N)$$

Previous value hold

$$F = G = E$$

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL = H), DA16 (PSSL = L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

(2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (-12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higher 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT = "1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	−12 dB	
0	1	−∞ dB	(See Note)
1	1	−12 dB	(See Note)

Note:

When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.

Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

8. Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 2.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
- **8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz**
- **DO OFF/ON: Digital out OFF/ON**
- **DF OFF/ON: Digital filter OFF/ON**
- **P/S: Parallel output/serial output**
- **OB/2's: Offset binary/2's complement**
- **CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio**

Table 2

- **Selection of clock**

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

- **Selection of digital filter (Refer to "9. Digital filter".)**

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

- **Selection of parallel output/serial output**

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) :
C1F2 (DA02) : Error correction status monitor output at C1 decode.
C2F1 (DA03) :
C2F2 (DA04) : Error correction status monitor output at C2 decode.
C2FL (DA05) : Correction status output, $C2FL = C2F1 \cdot C2F2$.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C210}}$ (DA14) : Bit clock (invert signal of $\overline{\text{C210}}$).
C210 (DA15) : Internal system clock (4.2336 MHz when DF is ON, 2.1168 MHz when CXD1125Q or DF is OFF).
DATA (DA16) : Serial data output (MSB or LSB first output)

• Selection of offset binary/2's complement

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

• Selection of CD ROM/audio compatibility

When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

9. Digital filter

The built-in digital filter has the following features:

1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

(1) Filter characteristics

Passing Band	Ripple from DC to 18 kHz	±0.07 dB max.
	Attenuation of 20 kHz with respect to 1 kHz	0.65 dB max.
Filtering Band	Attenuation of 44.1 ± 1 kHz with respect to 1 kHz	87 dB min.
	Attenuation of 44.1 ± 5 kHz with respect to 1 kHz	58 dB min.
	Attenuation of 44.1 ± 10 kHz with respect to 1 kHz	44 dB min.
	Attenuation of 44.1 ± 20 kHz with respect to 1 kHz	10 dB min.
	Frequency range in which attenuation is −30 dB with respect to 1 kHz	44.1 ± 14 kHz
	Frequency range in which attenuation is −60 dB with respect to 1 kHz	44.1 ± 4 kHz

10. Countermeasures to defect

To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK Pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin.

However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

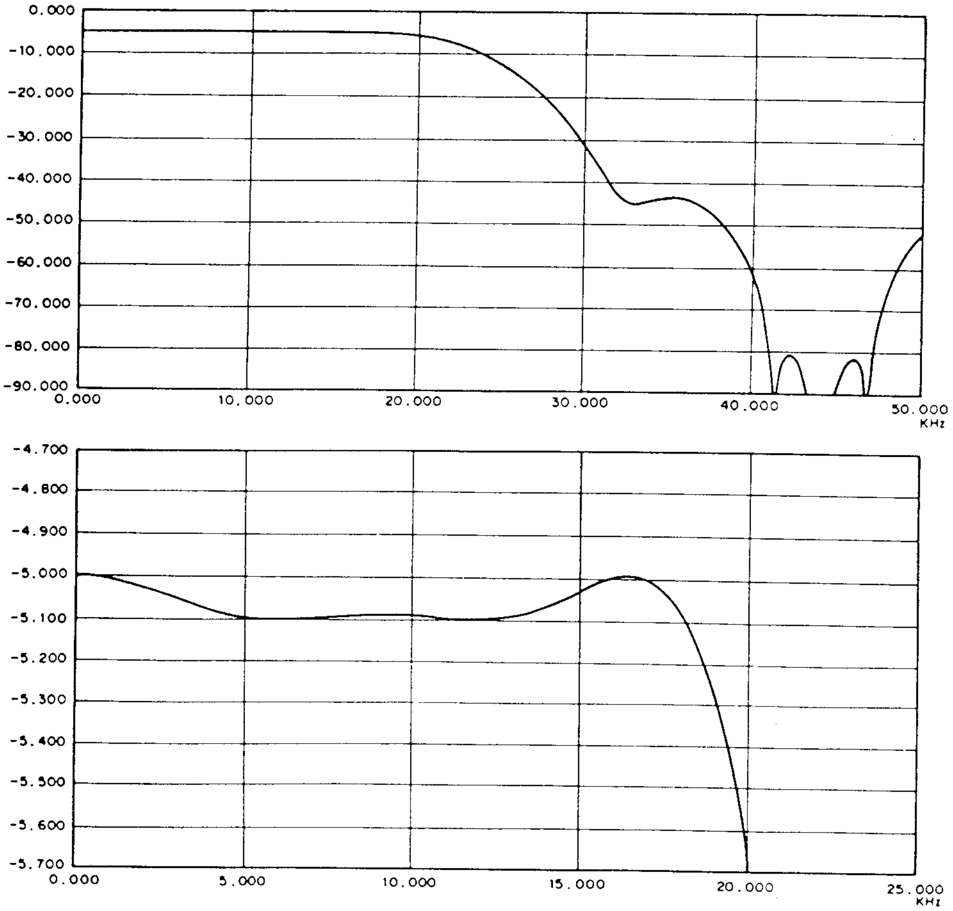
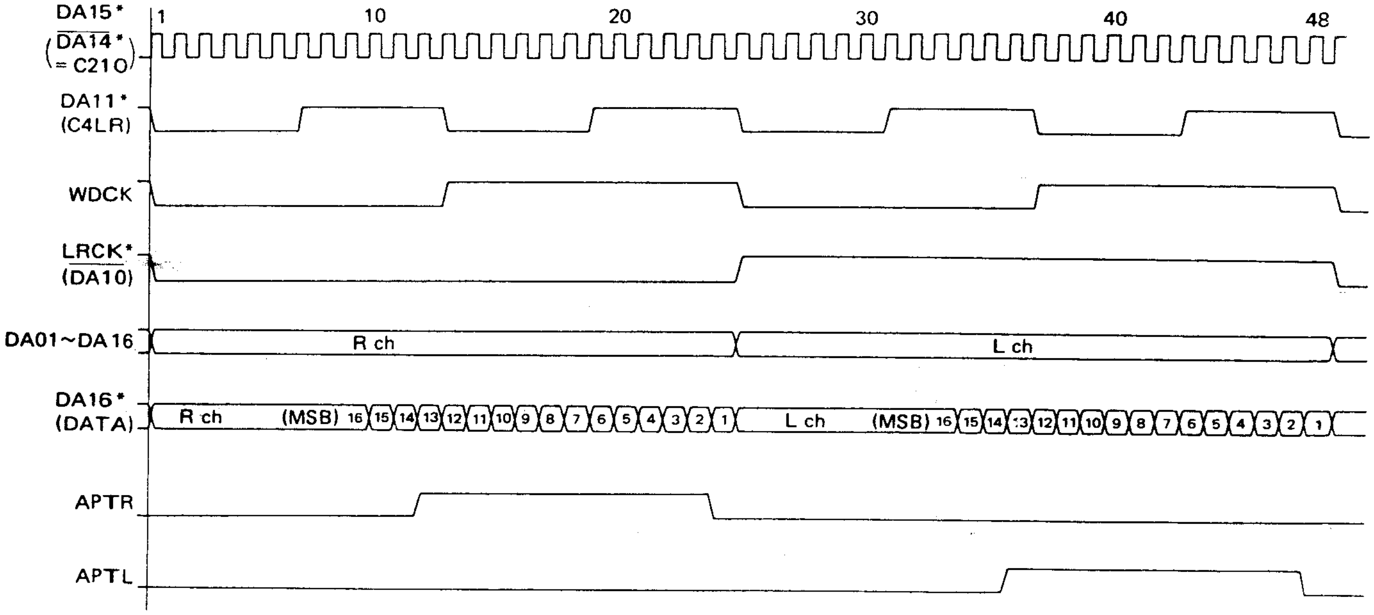


Fig. 14 Frequency characteristic after sample & hold

CIRCUIT DESCRIPTION

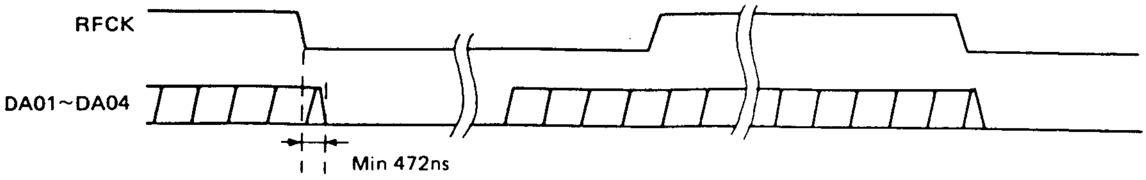
- **Timing chart**


DA15*
(DA14* = C210)
1
10
20
30
40
48
DA11*
(C4LR)
WDCK
LRCK*
(DA10)
DA01~DA16
R ch
L ch
DA16*
(DATA)
R ch
(MSB) 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
L ch
(MSB) 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
APTR
APTL

* When PSSL = "L".

Fig. 15 Timing chart of audio output

CIRCUIT DESCRIPTION


RFCK
DA01~DA04
Min 472ns

* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.

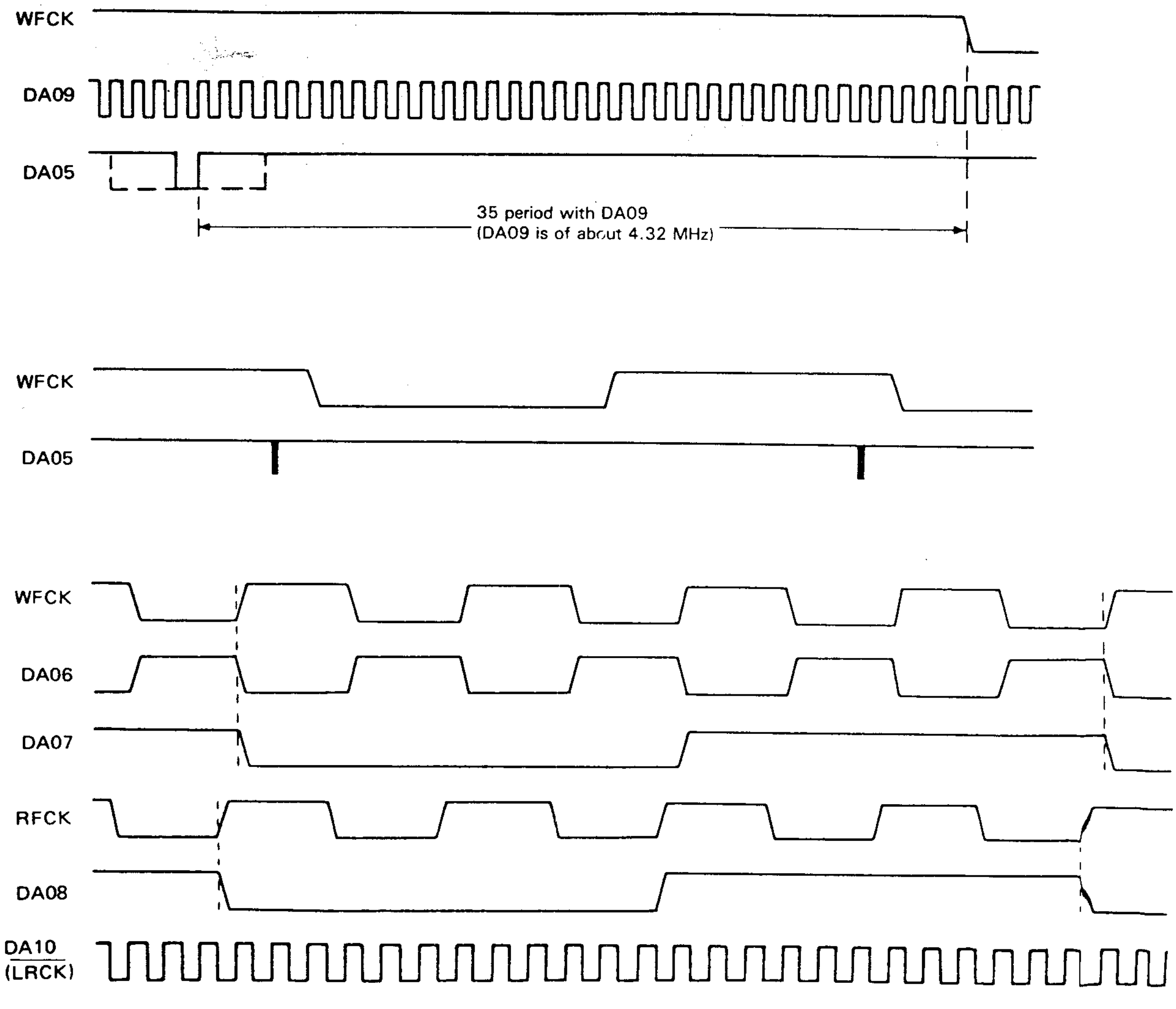

WFCK
DA09
DA05
35 period with DA09
(DA09 is of about 4.32 MHz)
WFCK
DA05
WFCK
DA06
DA07
RFCK
DA08
DA10
(LRCK)

Fig. 16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

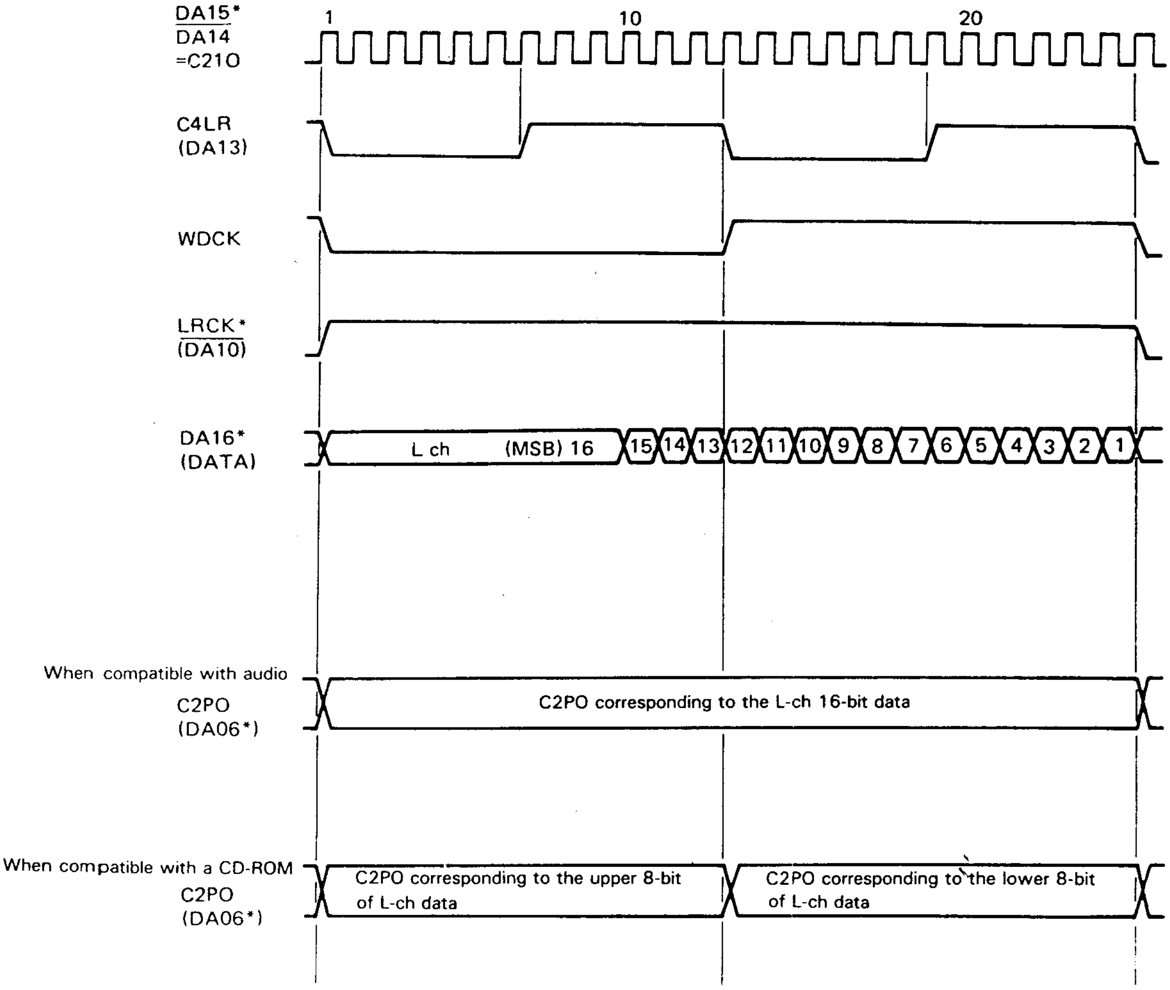

DA15*
DA14
=C21O
1
10
20
C4LR
(DA13)
WDCK
LRCK*
(DA10)
DA16*
(DATA)
L ch (MSB) 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
When compatible with audio
C2PO
(DA06*)
C2PO corresponding to the L-ch 16-bit data
When compatible with a CD-ROM
C2PO
(DA06*)
C2PO corresponding to the upper 8-bit of L-ch data
C2PO corresponding to the lower 8-bit of L-ch data

Fig. 17 Timing chart of C2PO output (when PSSL="L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

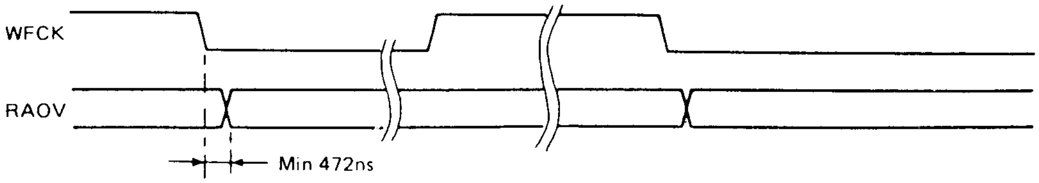

WFCK
RAOV
Min 472ns

Fig. 18 Timing chart of RAOV output

MECHANISM DESCRIPTION

1. Structure of mechanism

Roughly speaking, the mechanism consists of the following four sections.

(1) Section which loads, ejects and holds the cartridge.

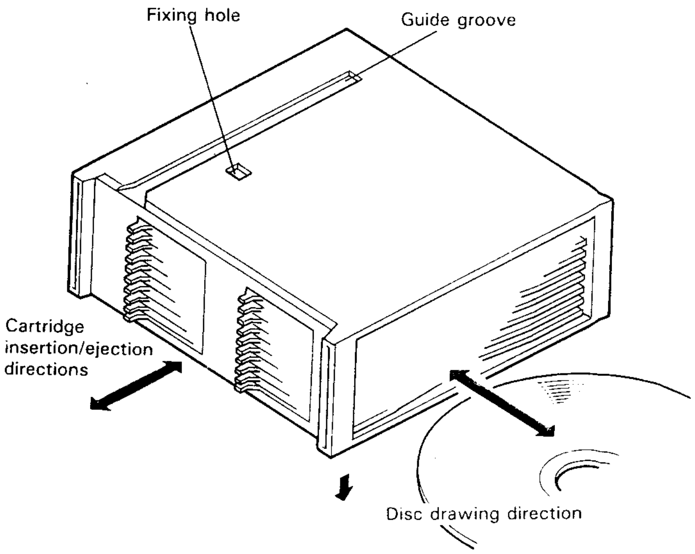
(2) Section which pulls out a disc from the cartridge and places it above the spindle motor. (This part also performs cartridge unloading, which consists of returning the disc to the specified position in the cartridge.)

(3) Section which moves up/down the section mentioned in (2), in order to place the disc on the turntable and to move it to the specified position of the cartridge when unloading it.

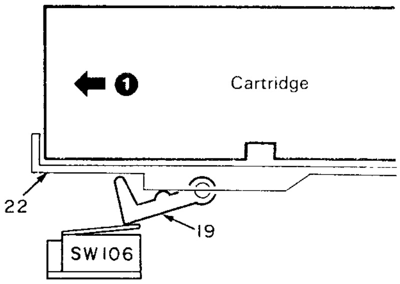
(4) Section consisting of the sled motor, spindle motor and pickup used for playing the disc.

2. Cartridge loading and ejection operations

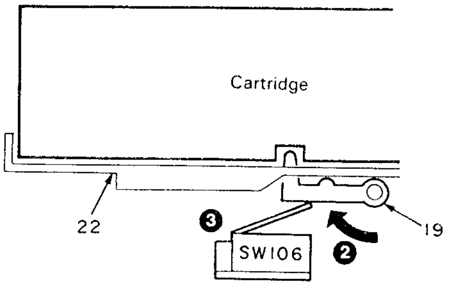
A guide groove and a square hole are located on the bottom side of the cartridge.



(1) When the cartridge is inserted, the projection on the mechanism (roller) is applied on the guide groove, guided by it and pushed in (❶).
When the projection is pushed in until the specified position, its hook is engaged with the position of the fixing hole so the cartridge is fixed (❷).

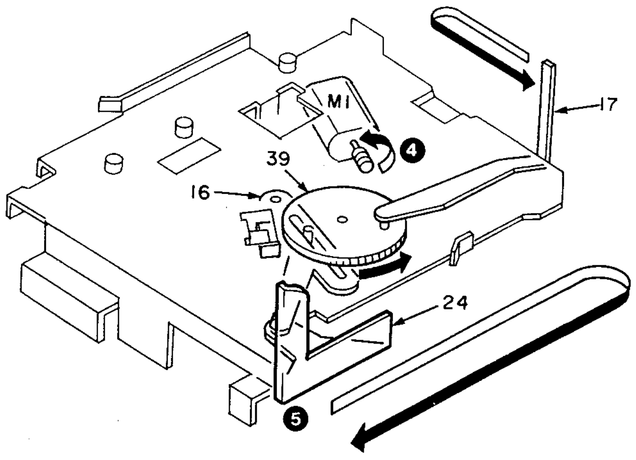


The cartridge insertion is a manual operation, and it is fixed by the hook which is moved up when the lever (22) is pushed. When the hook moves up, it turns ON a switch (SW106) interlocked with it and the presence of the cartridge is detected by the switch (❸).

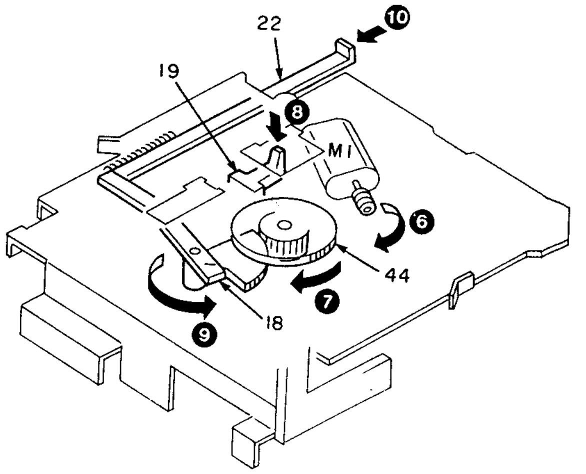


MECHANISM DESCRIPTION

When the switch (SW106) is turned ON for the first time, the motor (M1) rotates once in the CW direction (❹). This CW rotation of the motor (M1) causes the lever (16), which is used to place the disc completely inside the cartridge, to reciprocate once in front of the disc drawing slot on the cartridge (❺).



(2) The cartridge ejection is performed by the CCW rotation of the motor (M1) (❻). The motor rotation is transmitted to the cam (44) (❼), the hook (19) is disengaged from the fixing hole on the cartridge by the movement of the cam surface (❽), a force in the ejection direction is applied to the lever (22) by the Lever Ass'y (18) interlocked with the cam (❾), and the cartridge is pushed out (❿).



Functions of the motor and switches

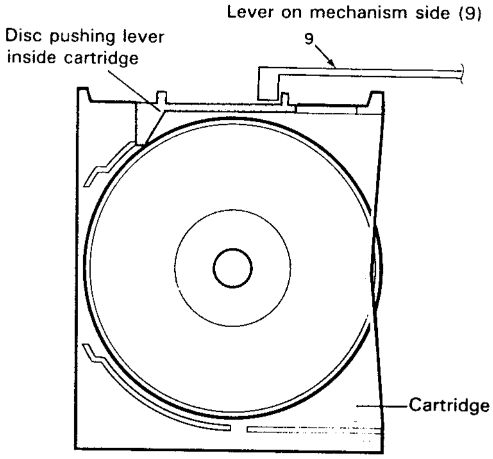
Motor (M1):	CW rotation moves the lever used to place the disc completely in the cartridge.
Switch (SW105):	Detects the home position of the lever (16) by means of the cam (39).
Motor (M1):	CCW rotation rotates the cam (44) used to push out the cartridge and disengage the hook.
Switch (SW106):	Detects the presence of cartridge (LOADING/EJECT).
Switch (SW107):	Detects the home position of the ejection cam.

MECHANISM DESCRIPTION

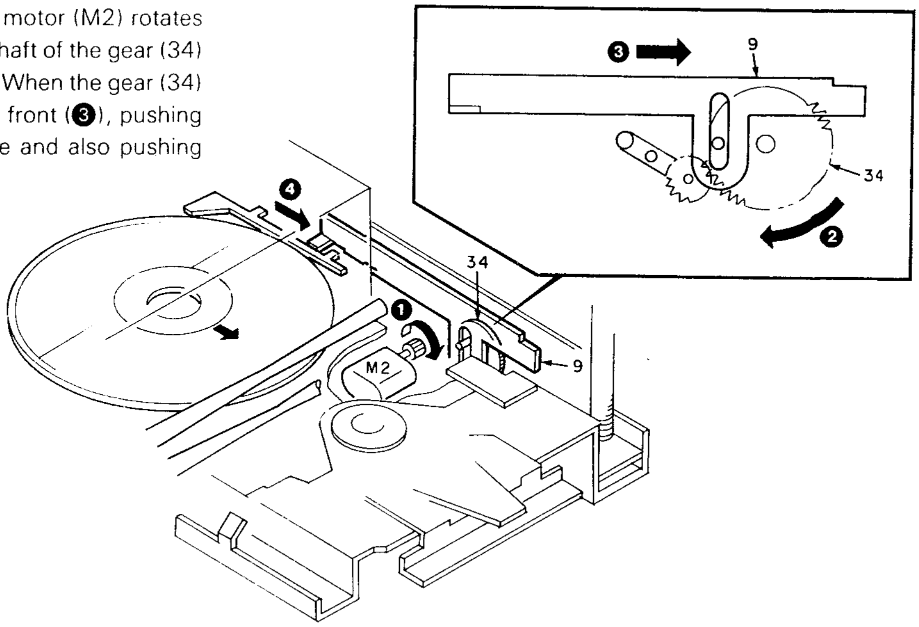
3. Disc loading and ejection with respect to the cartridge

A lever for pushing out the disc is located inside the cartridge, and two sections of the lever are projected outside the cartridge.

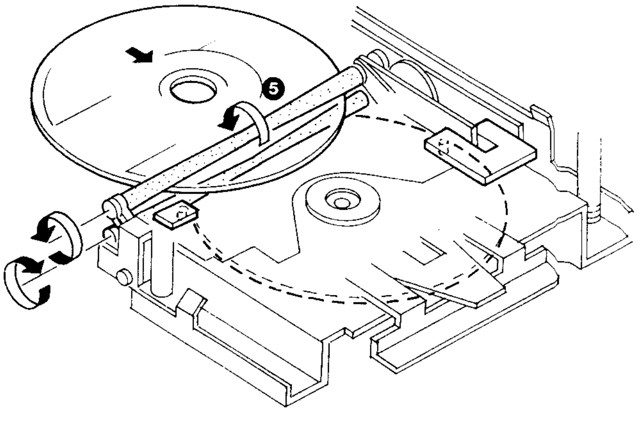
The lever (9) is placed in front of one of the projections. However, it can also move up/down when all discs are inside the cartridge or when a disc has been loaded on the mechanism.


Lever on mechanism side (9)
Disc pushing lever inside cartridge
9
Cartridge

For loading a disc on the mechanism, the motor (M2) rotates (❶), also rotating the gear (34) (❷). The shaft of the gear (34) is inserted in the long hole on the lever (9). When the gear (34) rotates, the lever (9) is pushed toward the front (❸), pushing the disc pushing lever inside the cartridge and also pushing the disc toward the front (❹).

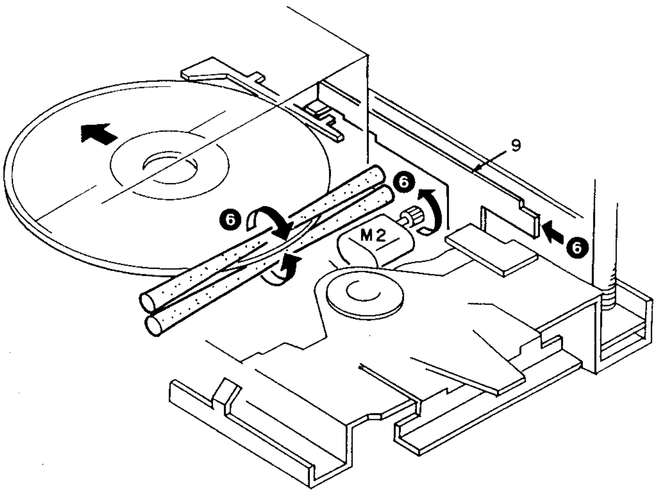


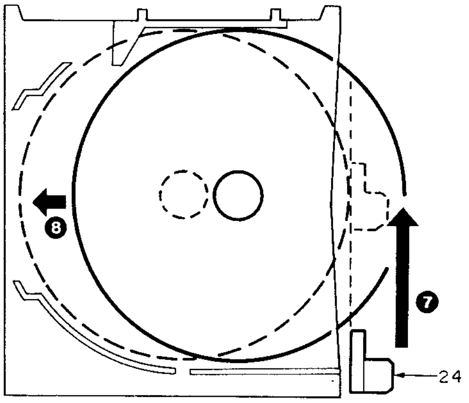
By means of a pair of rollers inside the mechanism which are rotated by the motor (M2), the disc is transported to the specified position with the same procedure as the KDC-80 and 90R (❺).



MECHANISM DESCRIPTION

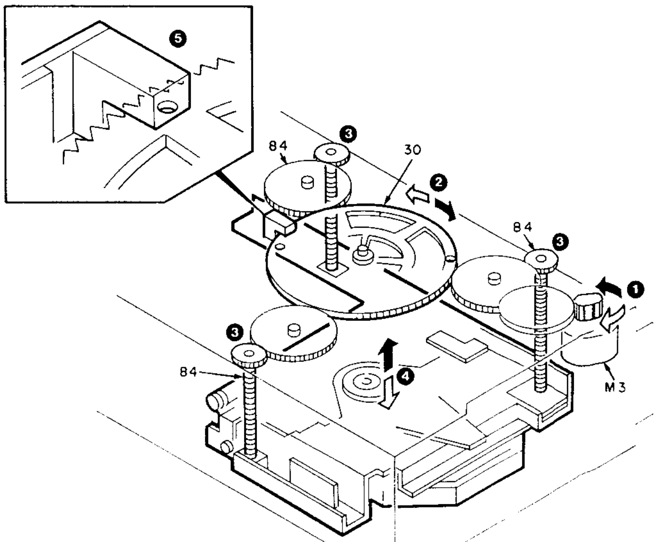
The disc is ejected from the mechanism to the cartridge in the reverse way to the above operations (❻). However, the lever (9) on the mechanism side moves only in one direction so it cannot return the disc pushing lever inside the cartridge. The disc pushing lever is returned by the disc itself. At the final stage on the rollers, it is pushed into the final position by the lever provided on the opening surface of cartridge (❼) (❽).
(Motor (M1) = CW, slider ass'y (24) moved)





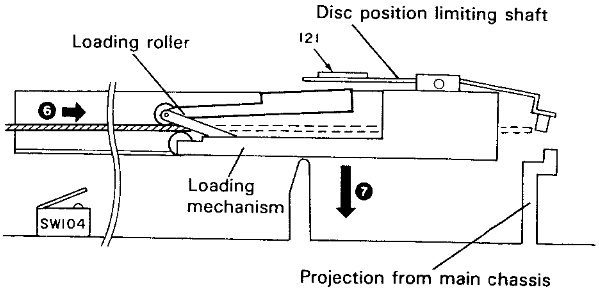
4. Up/down movement of loading mechanism

The initial position of the loading mechanism is the PLAY position, with which the disc is placed on the spindle.
The whole of the mechanism is moved up/down by the motor (M3) (❶), the rotation of which is transmitted through the gear (62) (❷), and to the 3 screws (84) (❸) (❹).
The loading positions of the 10 discs are detected by detecting the 2 holes of the gear (30) (❺).
(Motor (M3) CCW→holes detected).

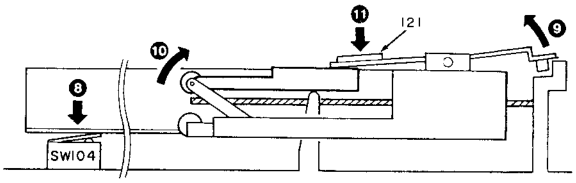


MECHANISM DESCRIPTION

After the disc is loaded in the specified position (❻), the loading mechanism moves down (❼), and enters the PLAY condition when the switch (SW104) is turned ON (❽). At this time, the disc insertion position limiting shaft (❾) and roller are separated up and down from the disc (❿).


Disc position limiting shaft
Loading roller
121
❻
Loading mechanism
❼
SW104
Projection from main chassis

The actual playback becomes possible when the plate (121) is attracted magnetically to the turntable on the spindle motor. For ejecting the disc, the loading mechanism is moved up by the loading and empty operation. The cartridge position is detected when the switch (SW102) is turned ON.
The optics system design such as the disc spindle is the same as the KDC-80 and 90R including the constants used.


⓫
121
❾
❿
❽
SW104

TROUBLESHOOTING

Other than the previous, the remote control unit displays various error indications to show the following messages. (Each indication blinks for 2 seconds.)

E-01: No disc magazine in the changer, or the magazine is not set completely.
E-02: No discs in the disc magazine.
E-03: The specified track is not present on the disc.
(Example: This appears when the 15th track is specified for a disc on which only 10 tracks are contained.)
E-04: Disc is too dirty.
Condensation has occurred on the disc, or water drops are on the disc.
Disc is set upside down.
E-05: PGM button is pressed with no program.
E-99: Operation incorrect due to something being defective.
Press the reset switch on the controller unit.
If the "E-99" indication does not disappear with this operation, consult your nearest KENWOOD Service Agent.

WAIT:
- When the temperature exceeds 60°C, the protection circuit is engaged to stop any operation. At this time, this indication will appear.
- Open a window or turn the air-conditioner ON to lower the temperature. After a while, this indication will go out.
- This indication also appears for several seconds when making connections, or when the reset button is pressed.
- If the "WAIT" indication does not disappear, the main changer unit may be disconnected.

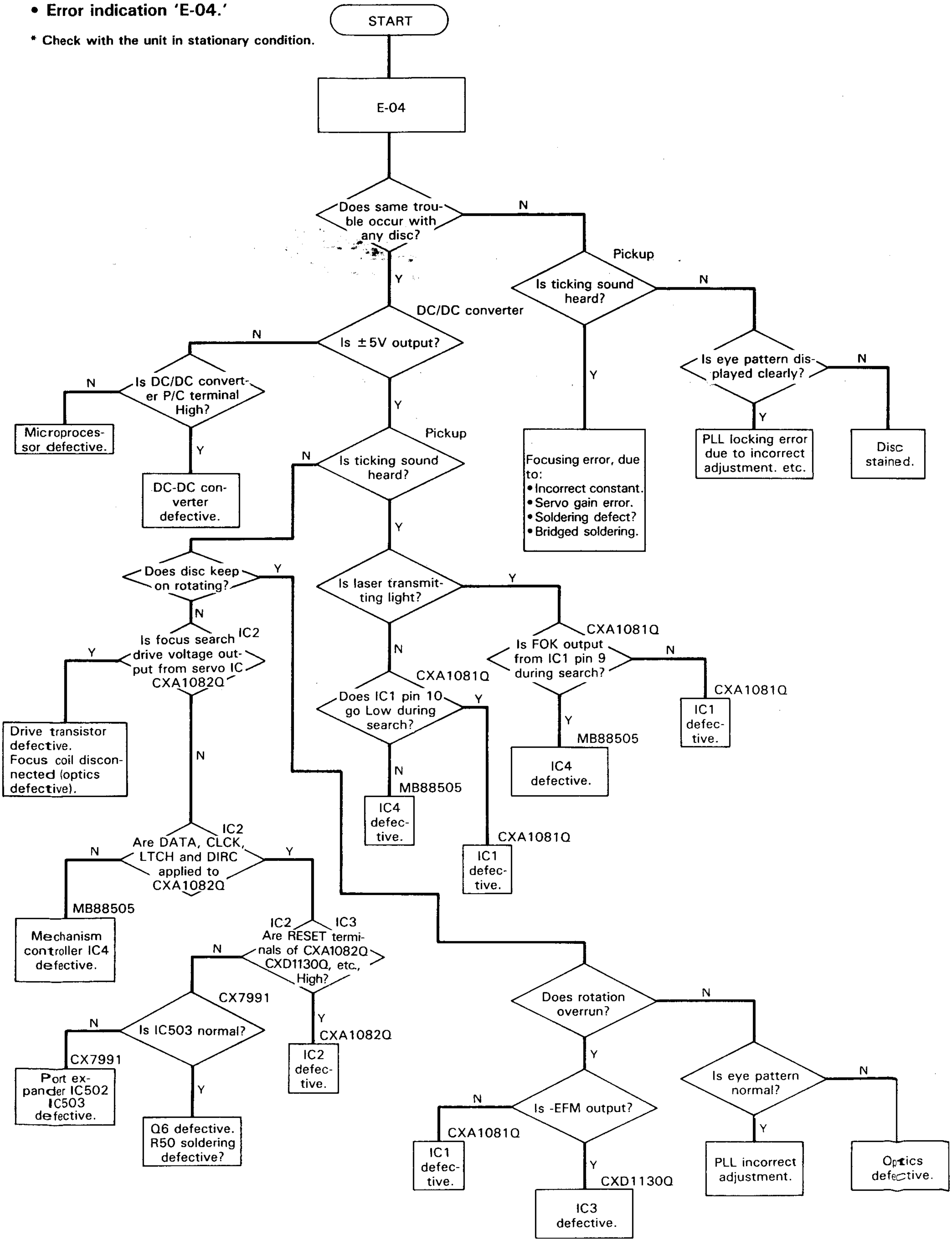
LOAD: This indication appears while a disc is being changed inside the changer.

* When no indicator appears in the controller and only illumination appears, the cable connector may nearly be disconnected.

TROUBLESHOOTING

- **Error indication 'E-04.'**

* **Check with the unit in stationary condition.**


START
E-04
Does same trouble occur with any disc?
N
Y
Pickup
Is ticking sound heard?
N
Y
Is eye pattern displayed clearly?
N
Y
PLL locking error due to incorrect adjustment. etc.
Disc stained.
Focusing error, due to:
• Incorrect constant.
• Servo gain error.
• Soldering defect?
• Bridged soldering.
DC/DC converter
Is ±5V output?
N
Is DC/DC converter P/C terminal High?
N
Microprocessor defective.
Y
DC-DC converter defective.
Y
Pickup
Is ticking sound heard?
N
Y
Does disc keep on rotating?
Y
N
IC2
Is focus search drive voltage output from servo IC CXA1082Q
Y
Drive transistor defective.
Focus coil disconnected (optics defective).
N
IC2
Are DATA, CLCK, LTCH and DIRC applied to CXA1082Q
N
MB88505
Mechanism controller IC4 defective.
Y
IC2
IC3
Are RESET terminals of CXA1082Q CXD1130Q, etc., High?
N
CX7991
Is IC503 normal?
N
CX7991
Port expander IC502 IC503 defective.
Y
Q6 defective. R50 soldering defective?
Y
CXA1082Q
IC2 defective.
Is laser transmitting light?
Y
CXA1081Q
Is FOK output from IC1 pin 9 during search?
N
CXA1081Q
IC1 defective.
Y
MB88505
IC4 defective.
N
CXA1081Q
Does IC1 pin 10 go Low during search?
Y
CXA1081Q
IC1 defective.
N
MB88505
IC4 defective.
Does rotation overrun?
N
Is eye pattern normal?
N
Optics defective.
Y
PLL incorrect adjustment.
Y
Is -EFM output?
N
CXA1081Q
IC1 defective.
Y
CXD1130Q
IC3 defective.

ADJUSTMENT

[LARGE ELEVATOR GEAR POSITION (LOCATION 10.5) ADJUSTMENT]

1. Move the middle elevator gear in the arrowed direction and place the top plate at the position where there are no clearances between the bottom face of the top plate and the top edges of the three claws.

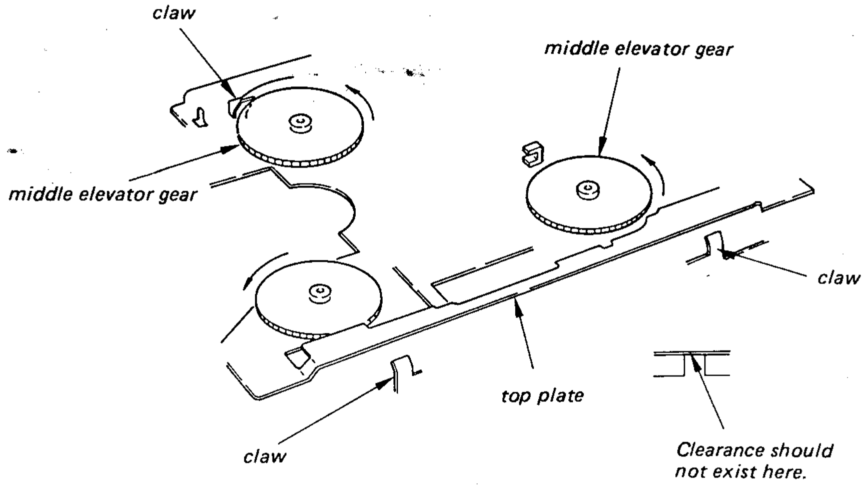
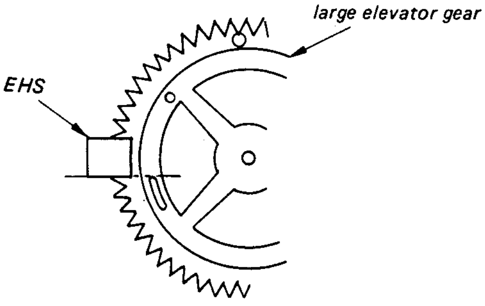

claw
middle elevator gear
middle elevator gear
claw
top plate
claw
Clearance should not exist here.

Fig. 1

2. Put the large elevator gear on the shaft of the top plate taking care not to move the middle elevator gears. The large elevator gear should be fastened by the top plate and EHS protrusion and should position in the relationship with the EHS as shown in Fig. 1.
3. After the placing, fix the large elevator gear with a retaining ring.


large elevator gear
EHS

Edge of EHS protrusion and edge of protrusion on the large elevator gear should be aligned as shown.

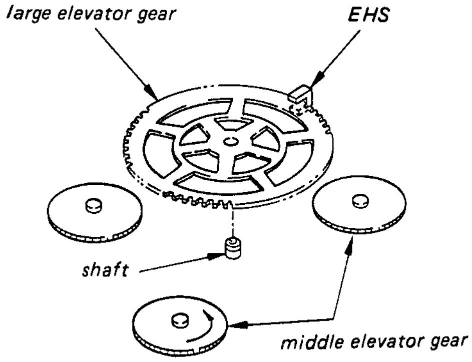

large elevator gear
EHS
shaft
middle elevator gear

Fig. 2

ADJUSTMENT

[HOMING ADJUSTMENT]

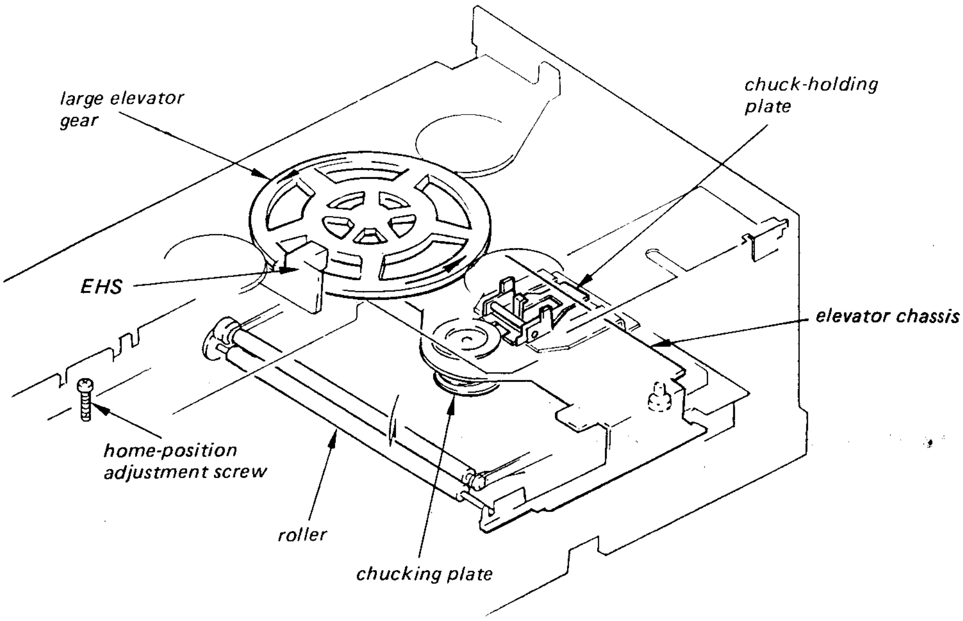

large elevator gear
chuck-holding plate
EHS
elevator chassis
home-position adjustment screw
roller
chucking plate

Fig. 3

1. Put the disk magazine containing several disks in the changer.
2. Initialize the changer.
3. Pull off the first disk.
4. Wait until the elevator lowers down to the home position.
5. Move the large elevator gear so that the clearance between the inner edge face of the chucking plate and edge of the top face of the stainless chuck-holding plate becomes in 1.5 mm (1/16 inches) as shown in Fig. 4.
6. Make a dot marking on the large elevator gear as shown in Fig. 5.
7. Re-put the first disk in the disk magazine.
8. Pull off the first disk again. The dot marking made in the step 6 above should position as shown in Fig. 5.
9. Fine adjust the position of the large elevator gear with the home-position adjustment screw shown in Fig. 3.

Adjustment Screw Position	Large Elevator Gear Position Displacement
One (1) turn in clockwise	15 (fifteen) degrees clockwise
One (1) turn in counterclockwise	15 (fifteen) degrees counterclockwise

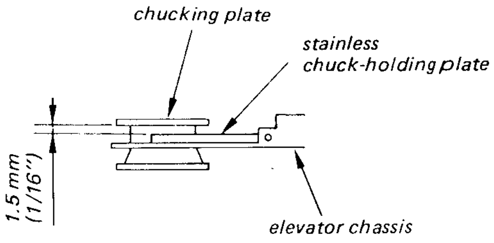
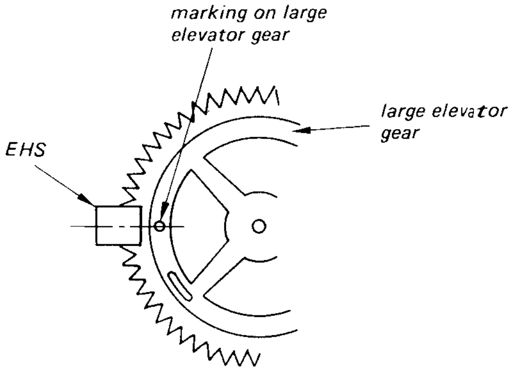

chucking plate
stainless chuck-holding plate
1.5 mm (1/16")
elevator chassis

Fig. 4


marking on large elevator gear
large elevator gear
EHS

Note:
Make a marking near and on the center line of the EHS sensor.

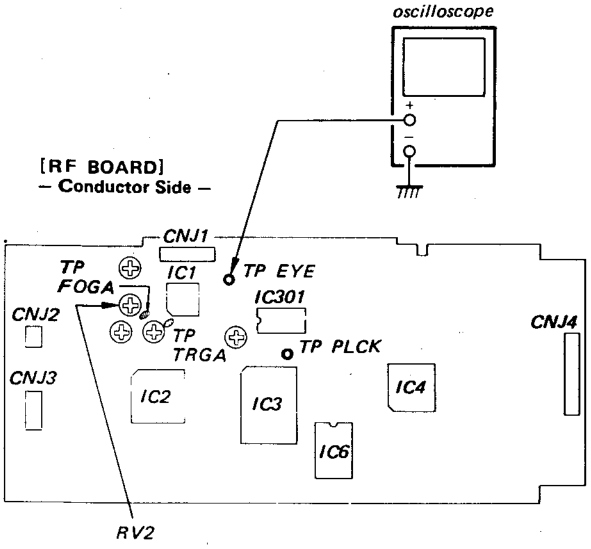
Fig. 5

ADJUSTMENT

1. Perform adjustments as given.
2. Be sure to use the disc "YEDS-18".
3. Unsolder the small shield plate from the RF board.
4. Power supply voltage: DC 14.4 V (more than 2A).

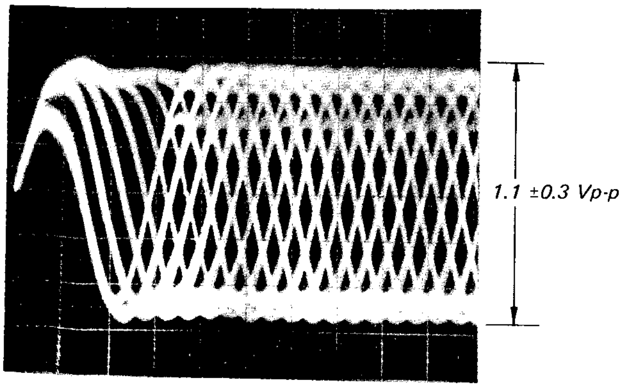
1. Focus Offset Adjustment

Procedure:


oscilloscope
+
–
[RF BOARD]
– Conductor Side –
CNJ1
TP FOGA
IC1
TP EYE
IC301
CNJ2
TP TRGA
TP PLCK
CNJ4
CNJ3
IC2
IC3
IC4
IC6
RV2

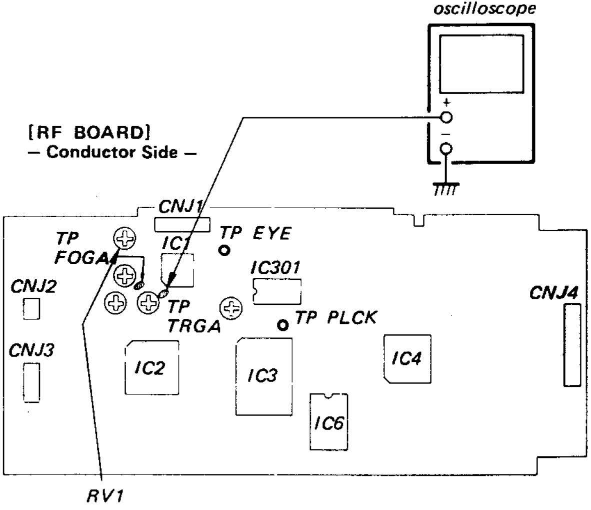
1. Connect the oscilloscope to RF board test point EYE.
2. Put the set into play mode by loading the disc.
3. Adjust main board RV2 so that the oscilloscope waveform eye pattern is good.
   (A good eye pattern means that the diamond shape (◇) in the center of the oscilloscope can be clearly distinguished.)

Volt/Div: 200 mV
Time/Div: 0.5 μSec



2. Tracking Offset Adjustment

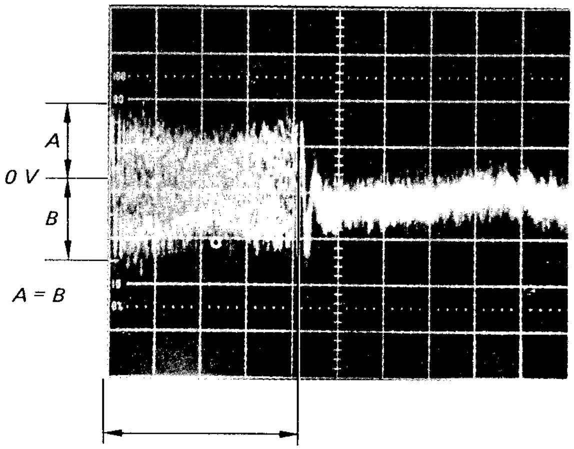
Procedure:


oscilloscope
+
–
[RF BOARD]
– Conductor Side –
CNJ1
TP FOGA
IC1
TP EYE
IC301
CNJ2
TP TRGA
TP PLCK
CNJ4
CNJ3
IC2
IC3
IC4
IC6
RV1

1. Connect the oscilloscope to RF board test point TRGA, pin ① of IC1.
2. Put the set into play mode by loading the disc.
3. Press the |◀◀ or ▶▶| (or ◀◀ , ▶▶) button, then check the traverse waveform*.
4. Adjust RV1 (main board) so that oscilloscope reading is symmetrical in relation to 0 V.

*Traverse waveform: This is the tracking error waveform appears when crossing the track.

Volt/Div: 0.5 V
Time Div: 2 mSec
Center 0 V



traverse wafeform
(100 track jump waveform)

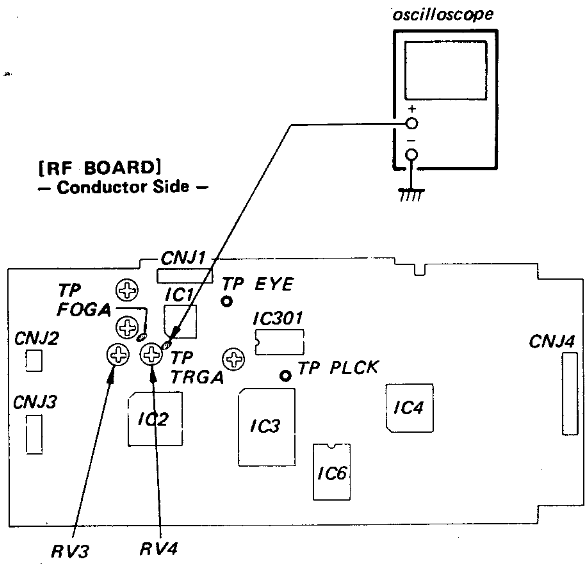
3. Tracking Gain Adjustment (coarse adjustment)

This adjustment is to be performed when replacing the following parts.

- Optical Pick-up Block
- RV4

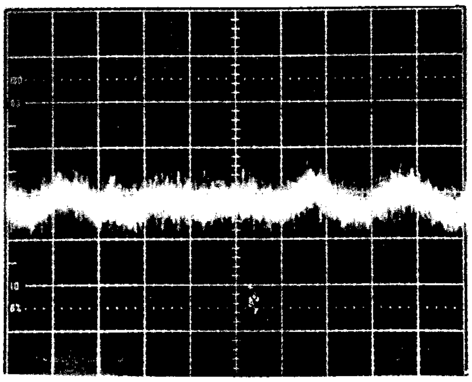
This adjustment should be performed after focus offset and tracking offset adjustments are completed.

Procedure:


oscilloscope
+
−
[RF BOARD]
– Conductor Side –
CNJ1
TP FOGA
IC1
TP EYE
IC301
CNJ2
TP TRGA
TP PLCK
CNJ4
CNJ3
IC2
IC3
IC4
IC6
RV3
RV4

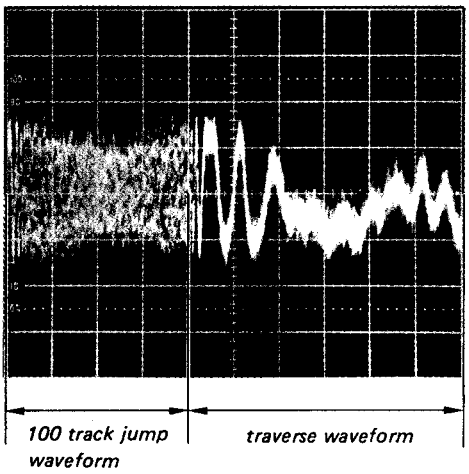
1. Connect the oscilloscope to RF board test point $\boxed{\text{TRGA}}$.
2. Put the set into play mode by loading the disc.
3. Turn RF board RV4 from clockwise stop, then check the oscilloscope waveform.
   Fix RV4 at the position where the waveform disappears.

Volt/Div: 0.5 V
Time/Div: 2 mSec

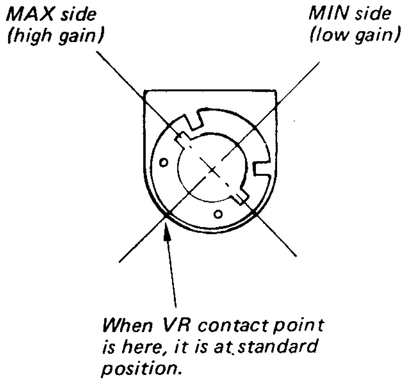


waveform when the wave appears

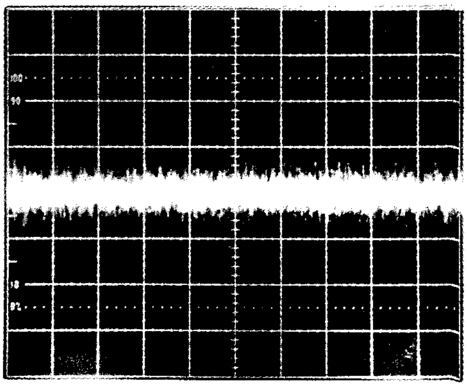
- **When gain is lowered . . .**
  When selecting by pressing |◀◀ or ▶▶| button, brake application is poor because of low tracking gain. Therefore, the traverse waveform appears after the 100 track jump waveform, then the selection will be located slowly.



- **When gain is highered . . .**
  Operation noise is heard due to a scratch or dust, then operation will be instability.


MAX side (high gain)
MIN side (low gain)
When VR contact point is here, it is at standard position.

RV3 standard position



waveform when the wave disappeared

ADJUSTMENT

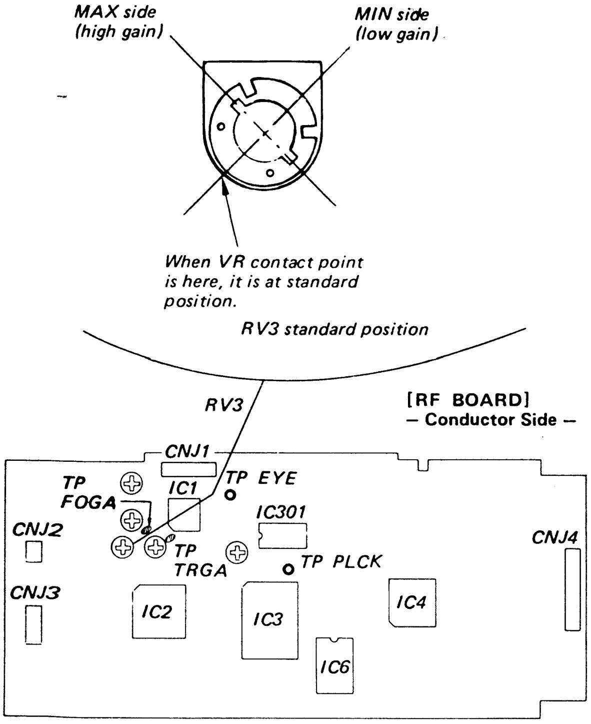
4. Focus Gain Adjustment (coarse adjustment)

This adjustment is to be performed when replacing the following parts.

- Optical Pick-up Block
- RV3

Procedure:

1. Set RV3 (RF board) to the standard position.
2. Check that there is not an abnormal amount of operation noise (white noise) from the 2-axis devise. If there is, turn RV3 slightly clockwise.

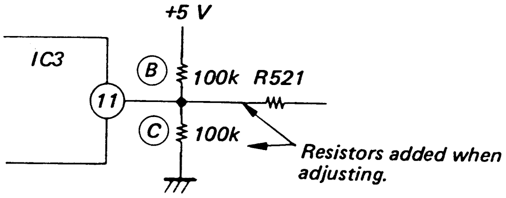

MAX side
(high gain)
MIN side
(low gain)
When VR contact point is here, it is at standard position.
R V3 standard position
RV3
[RF BOARD]
– Conductor Side –
CNJ1
TP
FOGA
IC1
TP EYE
IC301
CNJ2
TP
TRGA
TP PLCK
CNJ4
CNJ3
IC2
IC3
IC4
IC6

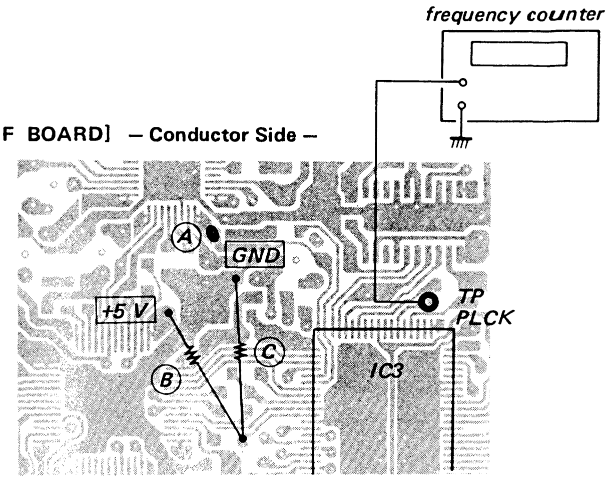
- **When gain is highered . . .**
  The set does not play because of no focus operation.
- **When gain is highered . . .**
  Operation noise is heard due to a scratch or a dust, then operation will be unstable.

5. PLL Freerun Frequency Adjustment

Procedure:

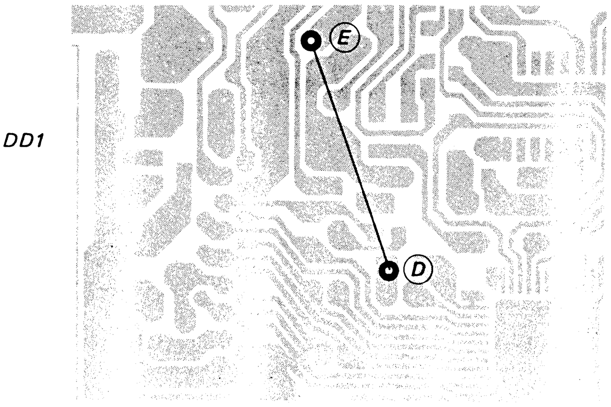
1. Unsolder the solder bridge at Ⓐ.
   (IC3 pin ⑤ is opened)
2. Connect 100 kΩ resistors to Ⓑ, Ⓒ.
   (This is to set the IC3 pin ⑪ voltage to 2.5 V)
3. Install a test jumper wire between Ⓓ and Ⓔ on the jack board to pull up the P/C terminal of the DC-DC converter ⊖.
4. Connect the frequency counter to RF board test point PLCK (IC3 pin ⑳).
5. Turn the power switch on (Do not use the disc), then adjust RV5 so that the frequency is 4.3218 MHz ±10 kHz.
6. After adjusting, reset 1, 2 and 3 as original.


+5 V
IC3
Ⓑ
100k
R521
11
Ⓒ
100k
Resistors added when adjusting.


frequency counter
Ⓐ
GND
+5 V
TP
PLCK
Ⓒ
Ⓑ
IC3

[RF BOARD] – Conductor Side –

[JACK BOARD] – Conductor Side –



VOLTAGE TABLES

CONTROLLER SECTION

IC801

1	4.6V
2	–
3	4.6V
4	4.9V
5	4.9V
6	4.9V
7	4.9V
8~16	–

IC802

1~28	–
29~32	4.6V
33	–
34~36	4.6V
37	–
38	4.6V
39~40	–
41	4.9V
42~45	–
46~53	–
54	4.9V
55~64	–
65	4.9V
66~67	–
68	4.8V
69~80	–

Q801

E	4.9V
C	8.4V
B	–

Q802

E	–
C	4.8V
B	–

Q803

E	–
C	–
B	–

HIDE-AWAY SECTION

IC101

1	4.4V
2	4.4V
3	1.6V
4	–
5	1.6V
6	4.2V
7	4.4V
8	8.3V

IC102

1~7	–
8	8.3V

IC201

1	4.4V
2	4.4V
3	1.6V
4	–
5	1.6V
6	4.4V
7	4.4V
8	8.3V

IC301

1	4.4V
2	4.4V
3	3.9V
4	–
5	3.9V
6	4.4V
7	4.4V
8	8.3V

IC302

1	–
2	4.2V
3	–
4	4.2V
5	4.1V
6	1.6V
7	–
8	4.2V
9	4.2V
10	–
11~14	4.2V
15	–
16	4.5V
17	0V
18	–
19	–
20	0V
21	4.8V
22	0V
23~29	4.2V
30	–
31~33	4.2V
34	–
35	4.2V
36	–
37	–
38~40	4.2V
41	–
42	7.6V
43	8.3V
44	–
45~47	4.2V
48	–

IC303

1~3	4.2V
4~7	–
8	8.3V

IC304

1	0V
2	4.8V
3	–

IC305

1~6	–
7	4.5V
8	4.6V
9~11	–
12	4.8V
13	–
14~21	–
22	4.8V
23	–
24	4.8V
25	4.8V
26	–
27	5.5V
28	–
29	4.9V
30~33	–
34	4.4V
35~40	–
41	4.8V
42	4.4V
43	0V
44	4.4V
45	–
46	–
47	4.8V
48	4.8V
49	4.6V
50	0V
51~53	–
54	0V
55	0V
56	4.5V
57	4.5V
58	4.8V
59~64	–

IC306

1	4.4V
2	–
3	–

Q101, Q102, Q201, Q202, Q305, Q306, Q315

E	–
C	–
B	–

Q301

E	–
C	14V
B	–

Q302

E	–
C	5.5V
B	–

Q303

E	–
C	14V
B	4.8V

Q304

E	8.3V
C	14V
B	–

Q310, Q312

E	–
C	–
B	4.8V

Q311

E	–
C	14.4V
B	–

Q313

E	14.4V
C	–
B	–

Q314

E	5.5V
C	14.4V
B	–

Q316

E	–
C	4.8V
B	–

Q319

E	8.4V
C	14V
B	–

Q401

E	–
C	–
B	2.4V

CHANGER SECTION

IC1

1	0V
2	–4.5V
3	0V
4	–0.4V
5	–0.5V
6	–
7	2.4V
8	2.4V
9	5V
10	0.1V
11	5V
12	–
13	0V
14	0.8V
15	0V
16	–
17	3V
18	–5V
19	0V
20	0V
21	–
22	0V
23	0V
24	–0.6V
25	–0.4V
26	–
27~29	–1.2V
30	–5.1V
31	–0.3V
32	0.1V

IC2

1	–
2~4	0V
5	1.2V
6~9	0V
10	5V
11	–0.1~0.2V
12	0V
13	0V
14	–0.1~0.5V
15	0V
16	–
17	–4V
18	5V
19	–5.1V
20	0.1V
21~25	5V
26	0V
27	2V
28	2.6V
29	2.2V
30	2.4V
31	3.8V
32	2.3V
33	5V
34	2.5V
35	5V
36	2.5V
37	5V
38	0V
39	0.8V
40	2.5V
41	–
42	0V
43	–5.1V
44	–4.5V
45~48	0V

IC3

1	0V
2	5V
3	2.5V
4	2.8V
5	2.4V
6	2.5V
7	5V
8	2.5V
9	2.2V
10	0V
11	1.7V
12	0V
13~16	5V
17	0.1V
18	5V
19	0V
20	5V
21	–
22	–
23	1.3V
24	0.1V
25	2.5V
26	–
27	–
28	5V
29~32	1.8V
33	5V
34~37	1.8V
38~40	2.5V
41~48	–2.5V
49	4.3V
50	2.7V
51	2.4V
52	–
53	0.2V
54	2.4V
55	–
56	5V
57~64	–

IC4

1~6	–
7~9	0V
10	–
11	–
12~16	5V
17	–
18	5V
19	–
20~29	5V
30	–
31~35	5V
36	2.4V

IC5

1	0V
2	5V
3	–0.3~0.3V
4	–5.1V
5~8	0V

IC6

1~8	2.5V
9~11	1.8V
12	0V
13~17	1.8V
18	2.7V
19	2.5V
20	2.7V
21	4.3V
22	2.5V
23	2.5V
24	5V

IC301

1	2V
2	4.3V
3	–
4	4.3V
5	0V
6~8	2.5V
9	2.4V
10	4.3V
11~13	–
14	4.3V
15~19	–
20	2V

IC302

1	0.2V
2	0.2V
3	0V
4	–5.1V
5	0V
6	0.2V
7	0.2V
8	5V

IC303

1	–0.3V
2	0V
3	–
4	–5.1V
5	–
6	0V
7	–0.3V
8	5V

IC501

1	14V
2	0V
3	0.4V
4	0.4V
5	0V
6	0.1V
7	14V
8	0V
9	0.4V
10	0.4V
11	0V
12	0.1V

IC502

1	4.5V
2	5V
3	–

IC503

1	0V
2	0V
3	–
4	0V
5	0V
6~8	–
9	4.8V
10~14	–
15	4.8V
16	0.4V
17	0V
18	0~5V
19	5V
20	4.8V

IC505

1~4	4.9V
5	0V
6~11	5V
12	–
13	5V
14	5V
15	0V
16	0.6V
17	5V
18	2.4V
19	0V
20	0V
21	5V
22	–
23	–
24	5V
25	5V
26	0.1V
27	0.1V
28	0.2V
29	0V
30	0.5V
31	0.1V
32	0.3V
33	–

IC507

1	14V
2	0V
3	0.4V
4~9	–
10	0.4V
11	0V
12	0.1V

Q1

E	4V
C	1.8V
B	3V

Q2

E	0.5V
C	–5V
B	1.2V

Q3

E	0.5V
C	5V
B	1.2V

Q4

E	0V
C	–5V
B	–0.1~0.2V

Q5

E	0V
C	5V
B	–0.1~0.2V

Q6, Q8

E	–
C	5V
B	0V

Q9

E	–
C	0V
B	2.7V

Q10

E	–
C	2.7V
B	0V

Q101, Q102 Q201, Q202

E	–
C	0V
B	–4.4V

Q301

E	5V
C	4.9V
B	–

Q302

E	–
C	–
B	0V

Q303

E	14V
C	–4.3V
B	14V

Q304

E	–
C	14V
B	0V

Q502

E	5V
C	0V
B	4.8V

Q505

E	4.8V
C	5V
B	4.9V

Q506

E	4.8V
C	0~5V
B	4.9V

Q511

E	0.3V
C	0.3V
B	0.3V

Q512

E	–
C	0V
B	5V

Q513

E	0.4V
C	0.3V
B	0.3V

Q514

E	–
C	0.3V
B	0V

Q515

E	0.3V
C	0.1V
B	0.3V

Q516

E	–
C	0V
B	0.7V

Q517

E	0.1V
C	0.1V
B	0V

Q518

E	–
C	0.3V
B	0.3V

Q519

E	–
C	0.1V
B	2.4V

Q520

E	0V
C	0V
B	0.1V

Q523

E	–
C	–
B	–

Q524

E	–
C	5V
B	–

Q704

E	–
C	0V
B	5V

Q705

E	14V
C	14V
B	13.4V

Q706

E	5V
C	13.5V
B	5.6V

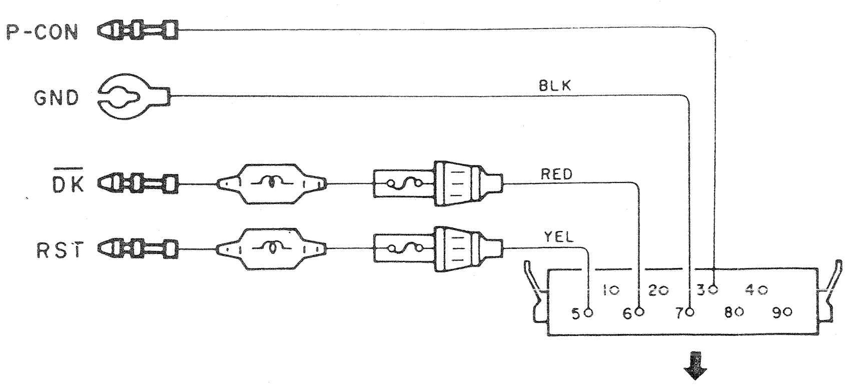
Q707

E	5.3V
C	14V
B	4.8V

Q710

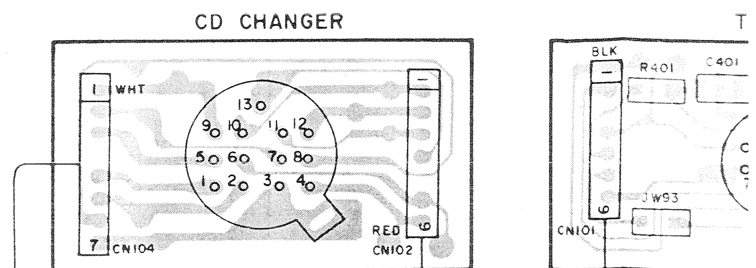
E	–
C	5V
B	0V

PC BOARD (Component side view)


P-CON
GND
$\overline{\text{DK}}$
RST
BLK
RED
YEL
10 20 30 40
50 60 70 80 90

1	N.C.
2	N.C.
3	P-CON
4	N.C.
5	RST
6	$\overline{\text{DK}}$
7	GND
8	N.C.
9	N.C.

1	ACC
2	B.UP
3	GND
4	DISP SELECT
5	SIGNAL. GND
6	CD RESET
7	SIGNAL.GND
8	MUTE
9	SIGNAL.L
10	DATA.IN
11	DATA. OUT
12	CLCK. IN
13	CLCK. OUT


CD CHANGER
WHT
RED
CN104
CN102
CN101
BLK
R401
C401
JW93

HIDE-AWAY SECTION

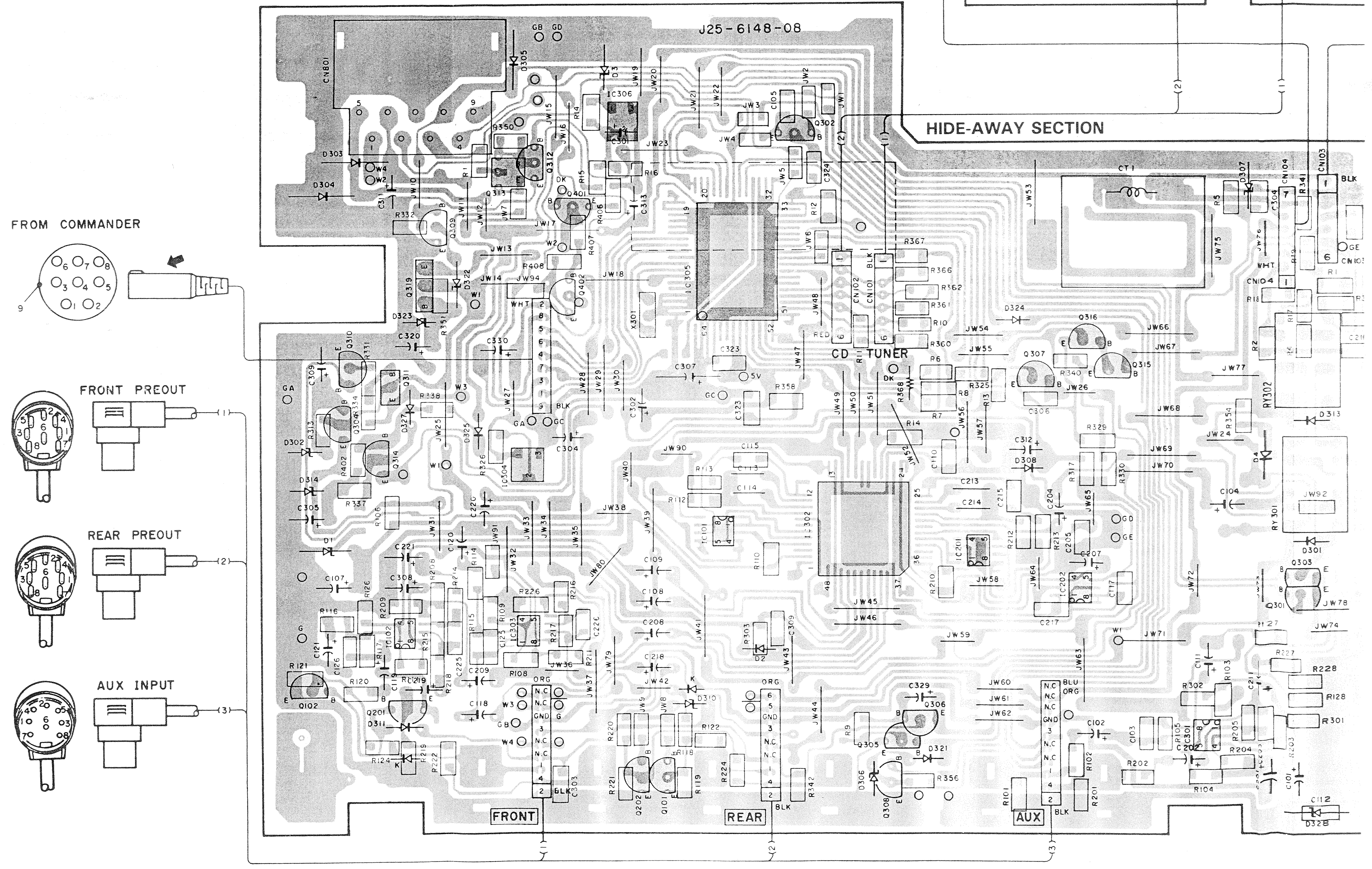
Ref. No.		Address
IC	Q	
	101	6F
	102	6D
	201	6E
	202	6F
	301	5J
	302	3G
	303	5J
	304	4E
	305	6H
	306	6H
	307	4H
	310	4E
	311	4E
	312	3F
	313	3F
	314	5E
	315	4I
	316	4I
	319	4E
	401	3F
101		5G
102		6E
201		5H
202		5I
301		6I
302		5G
303		6F
304		5F
305		3G
306		3F

1	S. DATA
2	$\overline{\text{RESET}}$
3	ACC 8.5V
4	CLK
5	REQ. OUT
6	$\overline{\text{POWER}}$
7	DATA
8	ILL
9	GND

1	Lch
2	GND
3	P-CONT
4	Rch
5	N.C.
6	N.C.
7	N.C.
8	N.C.

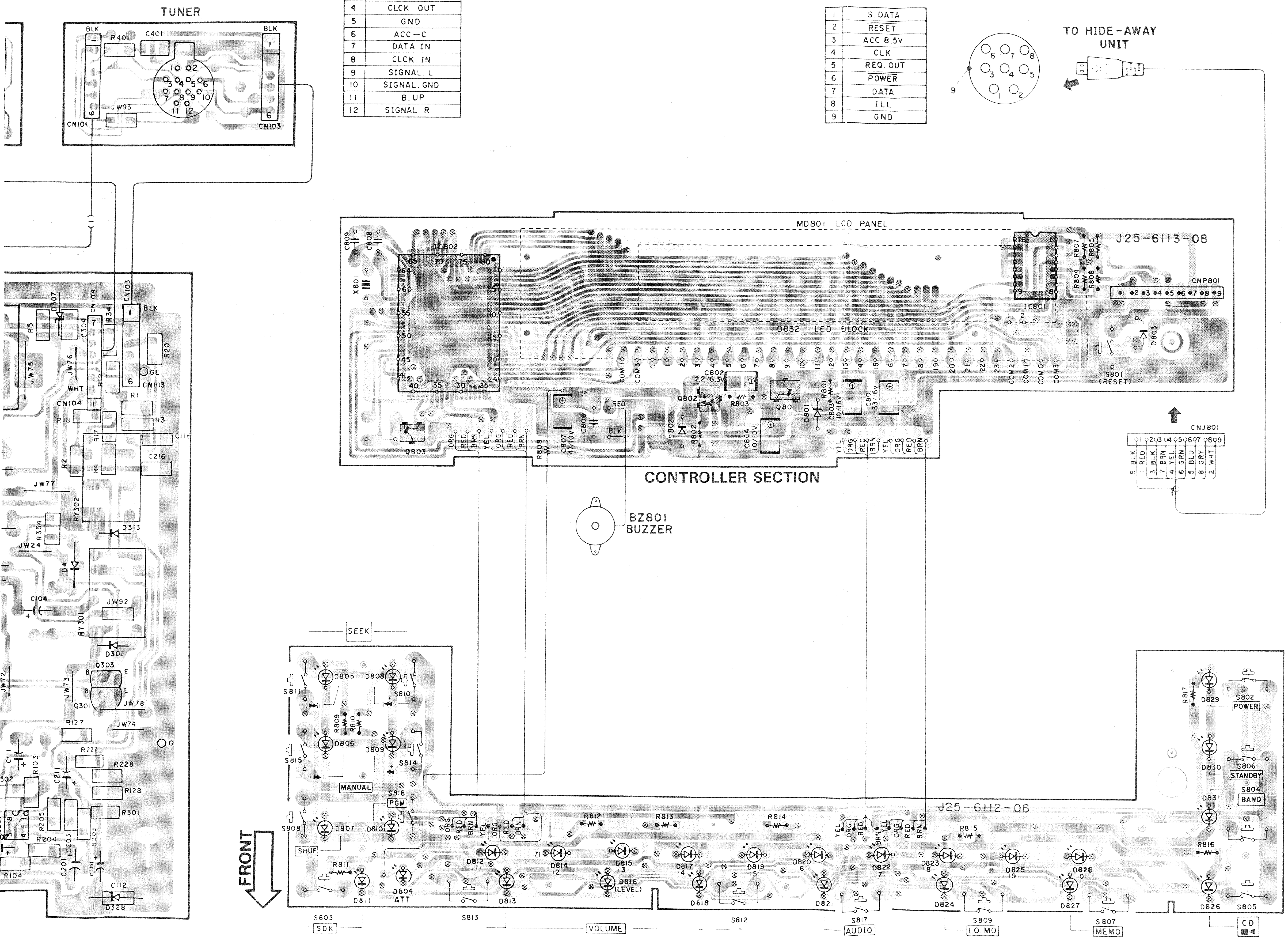
1	Lch
2	GND
3	P-CONT
4	Rch
5	RST
6	$\overline{\text{DK}}$
7	N.C.
8	N.C.

1	Lch
2	GND
3	P-CONT
4	Rch
5	N.C.
6	N.C.
7	N.C.
8	N.C.


FROM COMMANDER
FRONT PREOUT
REAR PREOUT
AUX INPUT
J25-6148-08
HIDE-AWAY SECTION
CN801
IC305
IC302
CD TUNER
CT1
RY301
RY302
FRONT
REAR
AUX
ORG
BLU
BLK
WHT
RED
(1)
(2)
(3)

1	DATA OUT
2	TUNER RESET
3	DISP SELECT
4	CLCK OUT
5	GND
6	ACC-C
7	DATA IN
8	CLCK IN
9	SIGNAL L
10	SIGNAL GND
11	B.UP
12	SIGNAL R

1	S DATA
2	RESET
3	ACC 8.5V
4	CLK
5	REQ OUT
6	POWER
7	DATA
8	ILL
9	GND


TUNER
BLK
R401
C401
CN101
JW93
CN103
TO HIDE-AWAY UNIT
MD801 LCD PANEL
J25-6113-08
IC802
IC801
CNP801
X801
C809
C808
D832 LED BLOCK
D803
S801 (RESET)
Q802
Q801
Q803
C802 2.2/6.3V
R803
R801
R802
D802
D801
C803 10/16V
C801 33/16V
C804 10/10V
C806
C807 47/10V
R808
CNJ801
9 BLK
1 RED
3 BLK
7 BRN
4 YEL
6 GRN
5 BLU
8 GRY
2 WHT
CONTROLLER SECTION
BZ801 BUZZER
SEEK
J25-6112-08
MANUAL
PGM
SHUF
ATT
(LEVEL)
POWER
STANDBY
BAND
SDK
VOLUME
AUDIO
LO MO
MEMO
CD
FRONT

CONTROLLER SECTION

Ref. No.		Address
IC	Q	
	801	3N
	802	3M
	803	4L
801		3O
802		3L

KDC-C100(K)

Refer to the schematic diagram for the values of resistors and capacitors.

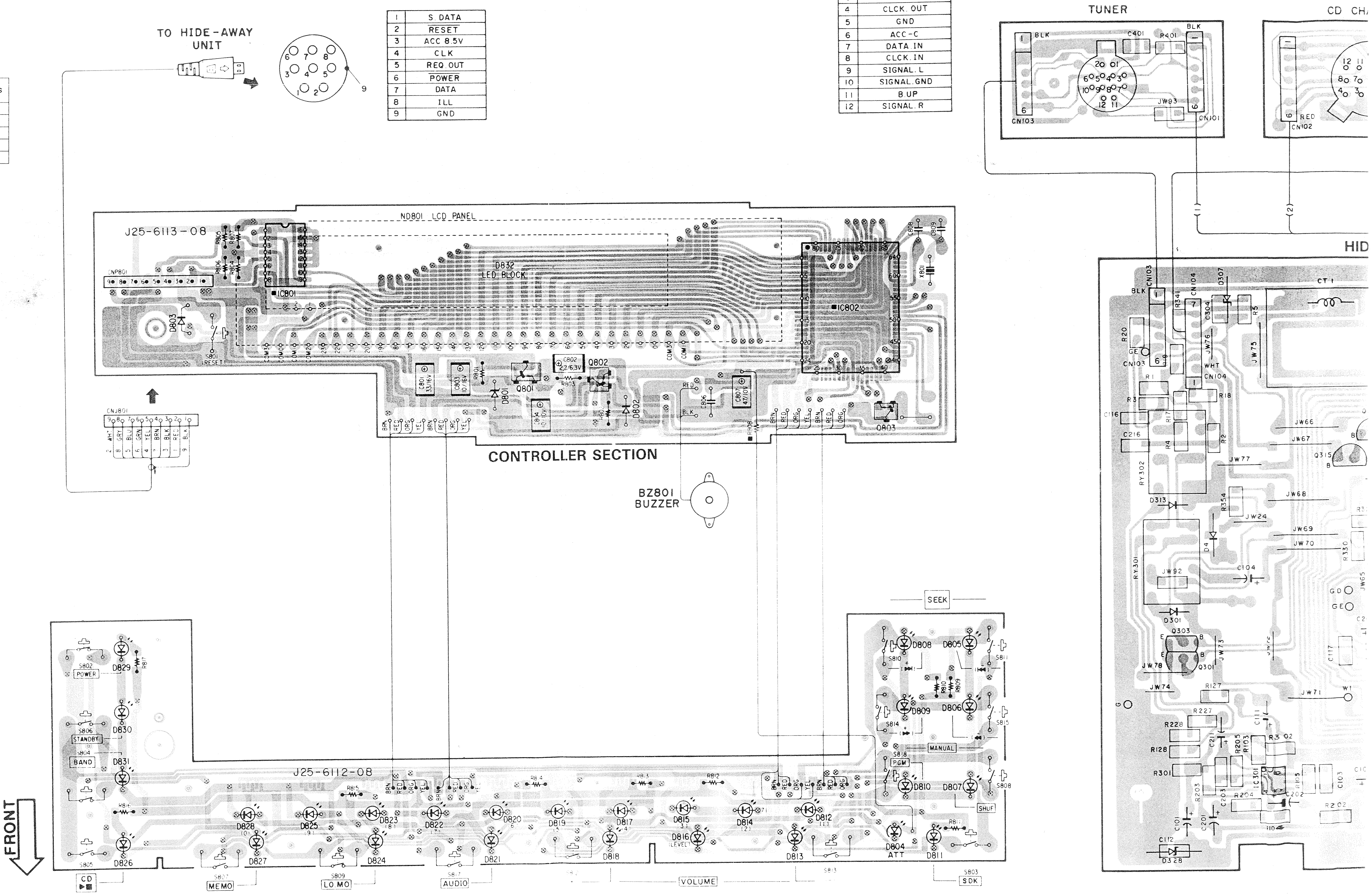
PC BOARD (Foil side view)

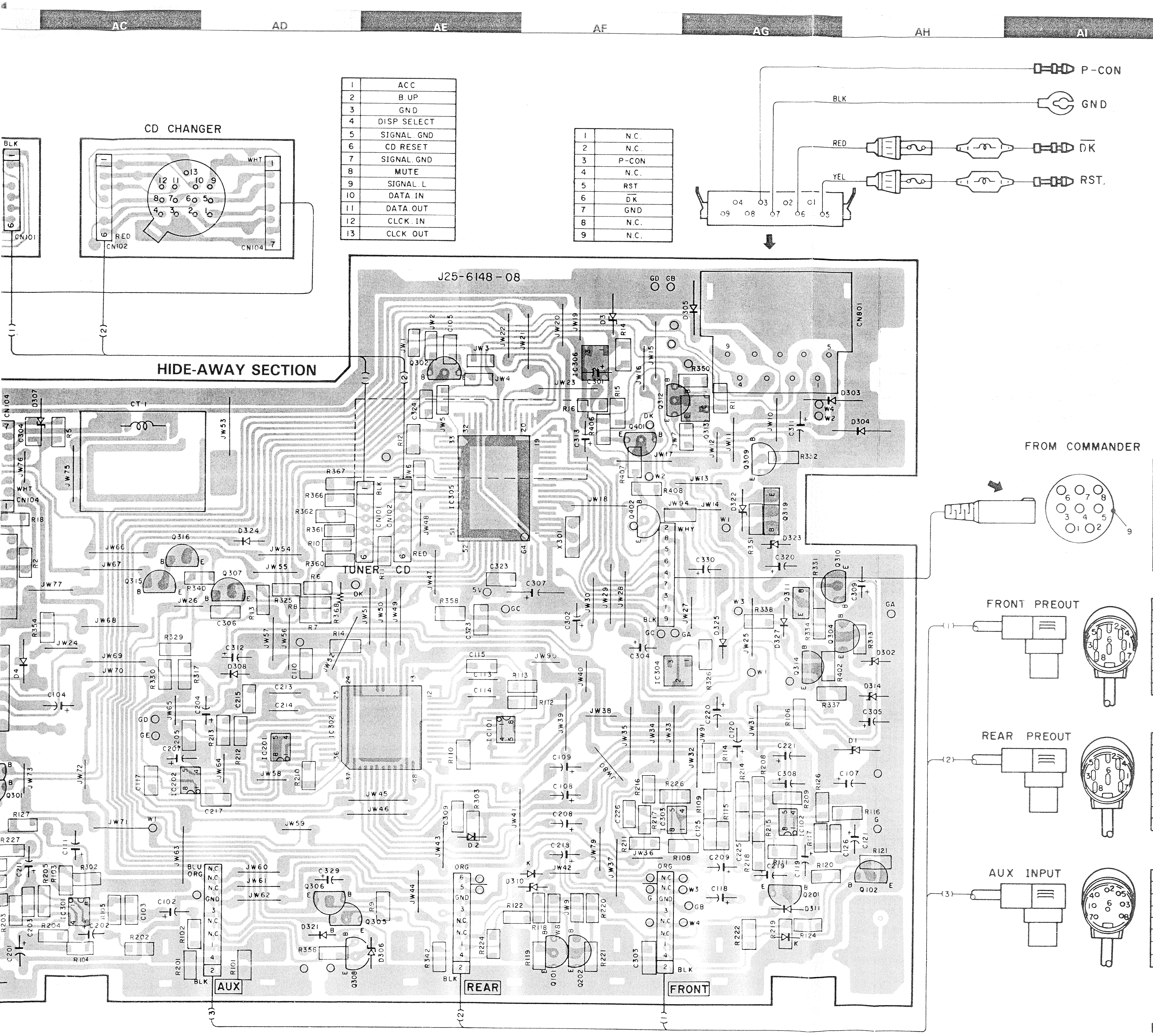
CONTROLLER SECTION

Ref. No.		Address
IC	Q	
	801	3X
	802	4Y
	803	4Z
801		3W
802		3Z

1	S. DATA
2	$\overline{\text{RESET}}$
3	ACC 8.5V
4	CLK
5	REQ. OUT
6	$\overline{\text{POWER}}$
7	DATA
8	ILL
9	GND

1	DATA. OUT
2	TUNER RESET
3	DISP. SELECT
4	CLCK. OUT
5	GND
6	ACC-C
7	DATA. IN
8	CLCK. IN
9	SIGNAL. L
10	SIGNAL. GND
11	B.UP
12	SIGNAL. R


TO HIDE-AWAY UNIT
9
TUNER
CD CH
HID
CN103
CN101
CN102
CN104
BLK
RED
WHT
C401
R401
JW93
J25-6113-08
ND801 LCD PANEL
D832 LED BLOCK
IC801
IC802
CNP801
CNJ801
D803
S801 RESET
C801 33/16V
C803 10/16V
R801
D801
Q801
C802 22/63V
R803
Q802
D802
C806
C807 47/10V
RED
BLK
Q803
X801
C808
C809
CONTROLLER SECTION
BZ801 BUZZER
SEEK
J25-6112-08
S802 POWER
D829
S806 STANDBY
D830
S804 BAND
D831
D826
S805
CD
D828
D827
S807 MEMO
D825
D823
D824
S809 LO.MO
D822
D821
S817 AUDIO
D820
D819
D818
D817
D815
D816 LEVEL
VOLUME
D814
D813
S813
D812
D804 ATT
D811
S803 SDK
D808
D805
S810
S811
D809
D806
S814
S815
MANUAL
S818 PGM
D810
D807
S808
SHUF
FRONT
CT1
RY301
RY302
Q301
Q303
Q315
D301
D313
D307
D328
D4
IC301
JW66
JW67
JW68
JW69
JW70
JW71
JW74
JW75
JW76
JW77
JW78
JW92
JW24
C104
C101
C112
C116
C117
C201
C202
C203
C211
C216
C304
R1
R2
R3
R4
R5
R17
R18
R20
R127
R128
R202
R203
R204
R205
R227
R228
R301
R330
R341
R354
GE
GD
G


AC
AD
AE
AF
AG
AH
AI
AJ
CD CHANGER
CN101
CN102
CN104
BLK
WHT
RED
HIDE-AWAY SECTION
J25-6148-08
CN801
P-CON
GND
DK
RST.
BLK
RED
YEL
FROM COMMANDER
FRONT PREOUT
REAR PREOUT
AUX INPUT
TUNER
CD
AUX
REAR
FRONT
IC101
IC102
IC201
IC202
IC301
IC302
IC303
IC304
IC305
IC306
CT1
X301

1	ACC
2	B.UP
3	GND
4	DISP SELECT
5	SIGNAL. GND
6	CD RESET
7	SIGNAL. GND
8	MUTE
9	SIGNAL. L
10	DATA. IN
11	DATA. OUT
12	CLCK. IN
13	CLCK OUT

1	N.C.
2	N.C.
3	P-CON
4	N.C.
5	RST
6	$\overline{\text{DK}}$
7	GND
8	N.C.
9	N.C.

FROM COMMANDER

1	S. DATA
2	$\overline{\text{RESET}}$
3	ACC 8.5V
4	CLK
5	REQ. OUT
6	$\overline{\text{POWER}}$
7	DATA
8	ILL
9	GND

FRONT PREOUT

1	Lch
2	GND
3	P-CONT
4	Rch
5	N.C.
6	N.C.
7	N.C.
8	N.C.

REAR PREOUT

1	Lch
2	GND
3	P-CONT
4	Rch
5	RST
6	$\overline{\text{DK}}$
7	N.C.
8	N.C.

AUX INPUT

1	Lch
2	GND
3	P-CONT
4	Rch
5	N.C.
6	N.C.
7	N.C.
8	N.C.

HIDE-AWAY SECTION

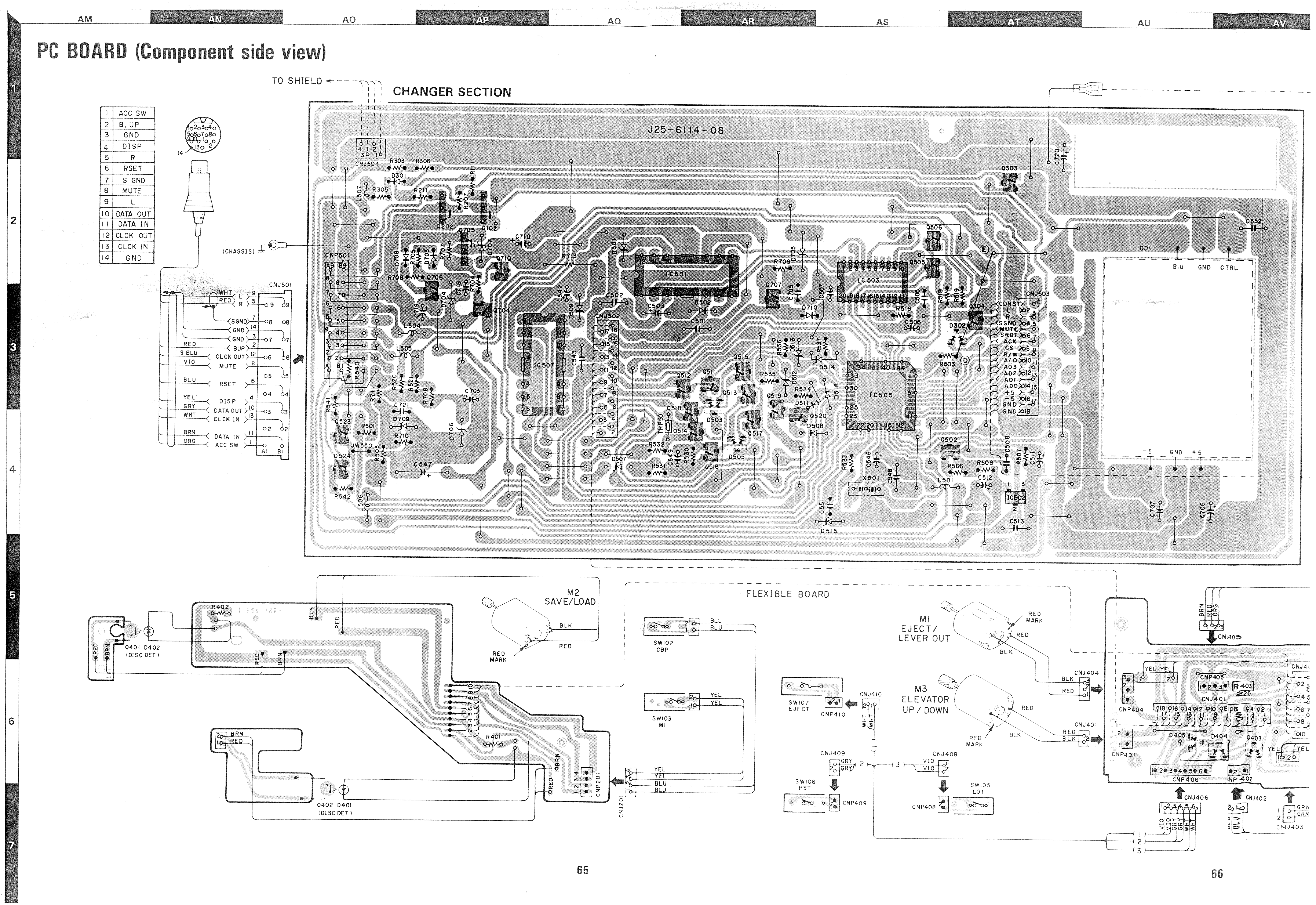
Ref. No.		Address
IC	Q	
	101	6AF
	102	5AH
	201	5AG
	202	6AF
	301	5AB
	302	3AE
	303	5AB
	304	4AH
	305	6AE
	306	6AD
	307	4AD
	310	4AG
	311	4AG
	312	3AF
	313	3AG
	314	4AG
	315	4AC
	316	4AC
	319	3AG
	401	3AF
101		5AE
102		5AG
201		5AD
202		5AC
301		6AC
302		5AE
303		5AF
304		5AG
305		3AE
306		3AF

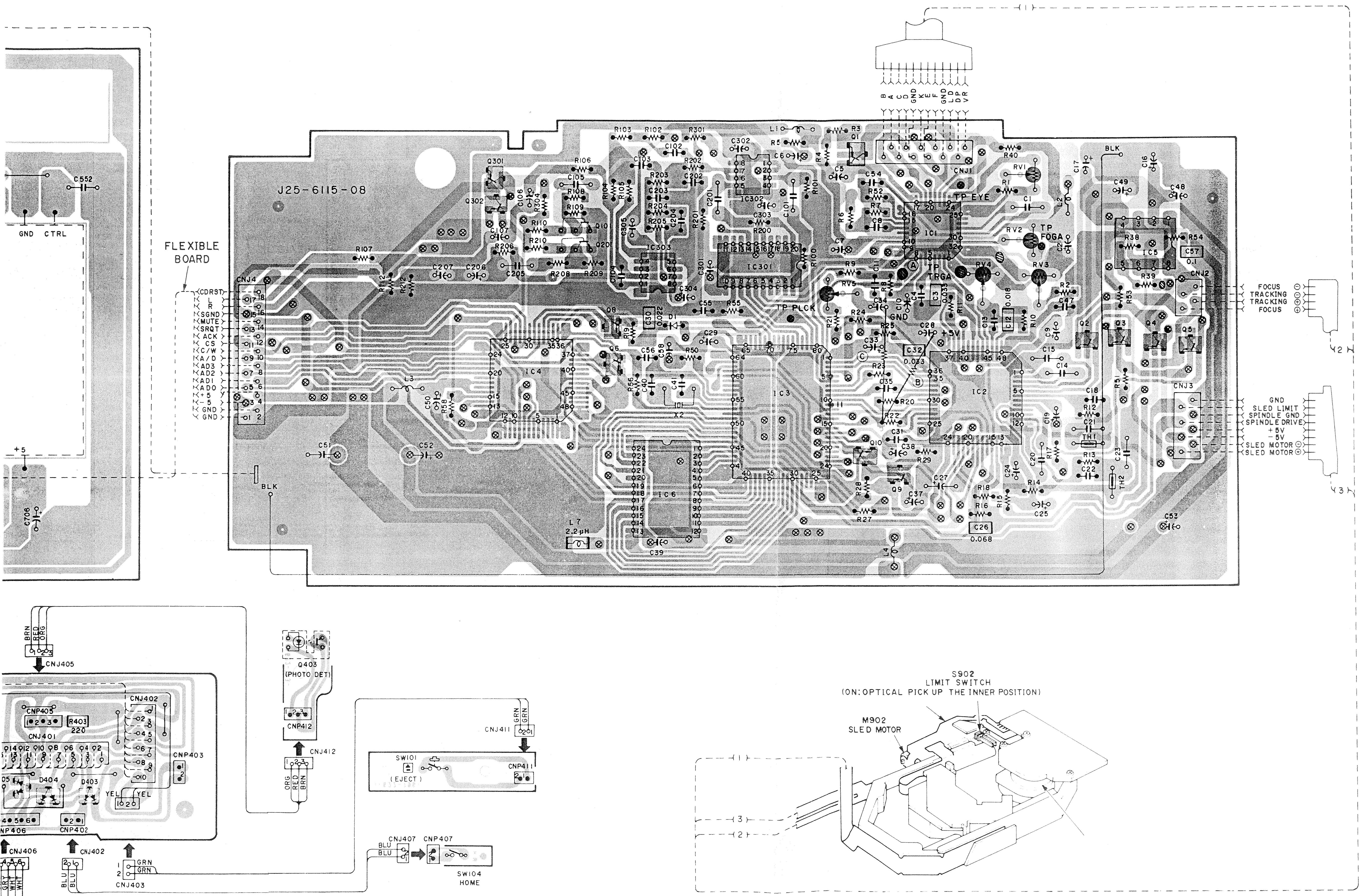
KDC-C100(K)

Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (Component side view)

1	ACC SW
2	B. UP
3	GND
4	DISP
5	R
6	RSET
7	S GND
8	MUTE
9	L
10	DATA OUT
11	DATA IN
12	CLCK OUT
13	CLCK IN
14	GND


AM
AN
AO
AP
AQ
AR
AS
AT
AU
AV
1
2
3
4
5
6
7
TO SHIELD
CHANGER SECTION
J25-6114-08
14
(CHASSIS)
CNJ501
WHT
RED
L
R
(SGND)
GND
GND
RED
BUP
S BLU
CLCK OUT
VIO
MUTE
BLU
RSET
YEL
DISP
GRY
DATA OUT
WHT
CLCK IN
BRN
DATA IN
ORG
ACC SW
A1
B1
CNP501
CNJ504
R303
R306
D301
R211
R207
R305
L507
Q202
Q102
Q705
D701
D708
R705
D703
R707
Q710
R706
Q706
C718
R704
D704
C719
Q704
L504
L505
C710
R713
D301
IC501
C502
C503
D502
C501
CNJ502
IC507
C543
C542
D509
R541
Q523
R501
R520
R521
R708
C721
D709
R710
C703
D706
R540
JW550
R505
Q524
C547
R542
L506
R709
D705
Q707
C705
C507
D710
IC503
Q506
Q505
R516
C506
C505
R518
R519
Q304
D302
R503
CNJ503
CDRST
SGND
MUTE
SRQT
ACK
CS
R/W
A/D
AD3
AD2
AD1
AD0
+5
-5
GND
Q303
C720
C552
DD1
B.U
GND
CTRL
Q515
Q512
Q511
Q513
R535
R534
D511
R533
D513
R537
D512
D514
Q519
D518
Q518
Q520
IC505
THP501
Q514
D503
Q517
D508
R532
C549
R530
R531
D507
Q516
D505
R533
C546
X501
C548
C551
D515
Q502
R506
R508
C508
R507
C511
L501
C512
IC502
C513
C707
C706
-5
GND
+5
(E)
(D)
M2
SAVE/LOAD
BLK
RED
RED MARK
R402
Q401 D402
(DISC DET)
RED
BRN
BLK
RED
R401
BRN
RED
CNP201
CNJ201
Q402 D401
(DISC DET)
FLEXIBLE BOARD
SW102
CBP
BLU
SW103
M1
YEL
SW107
EJECT
CNP410
CNJ410
WHT
CNJ409
GRY
SW106
PST
CNP409
CNJ408
VIO
SW105
LOT
CNP408
M1
EJECT/
LEVER OUT
RED MARK
M3
ELEVATOR
UP / DOWN
CNJ404
CNJ401
CNJ405
ORG
CNP405
R403
220
CNJ401
CNP404
CNP401
D405
D404
D403
CNP406
CNJ406
CNP402
CNJ402
CNJ403
GRN
YEL


J25-6115-08
FLEXIBLE BOARD
CDRST
L
R
SGND
MUTE
SRQT
ACK
CS
C/W
A/D
AD3
AD2
AD1
AD0
+5
-5
GND
GND
CNJ4
CNJ1
CNJ2
CNJ3
IC1
IC2
IC3
IC4
IC5
IC6
IC301
IC302
IC303
TP EYE
TP FOGA
TP TRGA
TP PLCK
BLK
C552
GND
CTRL
+5
C706
B A C GND K E F GND LD DP VR
FOCUS ⊖
TRACKING ⊖
TRACKING ⊕
FOCUS ⊕
GND
SLED LIMIT
SPINDLE GND
SPINDLE DRIVE
+5V
-5V
SLED MOTOR ⊖
SLED MOTOR ⊕
L7 2.2 μH
C26 0.068
C32 0.033
C57 0.1
S902
LIMIT SWITCH
(ON: OPTICAL PICK UP THE INNER POSITION)
M902
SLED MOTOR
Q403
(PHOTO DET)
CNJ405
CNJ402
CNP405
R403 220
CNJ401
CNP403
D404
D403
YEL
YEL
CNP406
CNP402
CNJ406
CNJ402
CNJ403
CNP412
CNJ412
CNJ411
SW101
(EJECT)
CNP411
CNJ407
CNP407
SW104
HOME
BRN RED ORG
ORG RED BRN
GRN GRN
BLU BLU
GRY WHT WHT

CHANGER SECTION-1

Ref. No.		Address
IC	Q	
	102	2AP
	202	2AP
	303	2AT
	304	3AT
	502	4AT
	505	2AS
	506	2AS
	511	3AR
	512	3AR
	513	3AR
	514	4AR
	515	3AR
	516	4AR
	517	3AR
	518	3AR
	519	3AR
	520	3AR
	523	4AO
	524	4AO
	704	3AP
	705	2AP
	706	2AP
	707	3AR
	710	2AP
501		2AR
502		4AT
503		2AS
505		3AS
507		3AP

CHANGER SECTION-2

Ref. No.		Address
IC	Q	
	1	2BA
	2	3BB
	3	3BC
	4	3BC
	5	3BC
	6	3AY
	8	3AY
	9	4BA
	10	4BA
	101	2AY
	201	2AY
	301	2AX
	302	2AX
1		2BA
2		3BB
3		3AZ
4		3AY
5		2BC
6		4AZ
301		2AZ
302		2AZ
303		2AZ

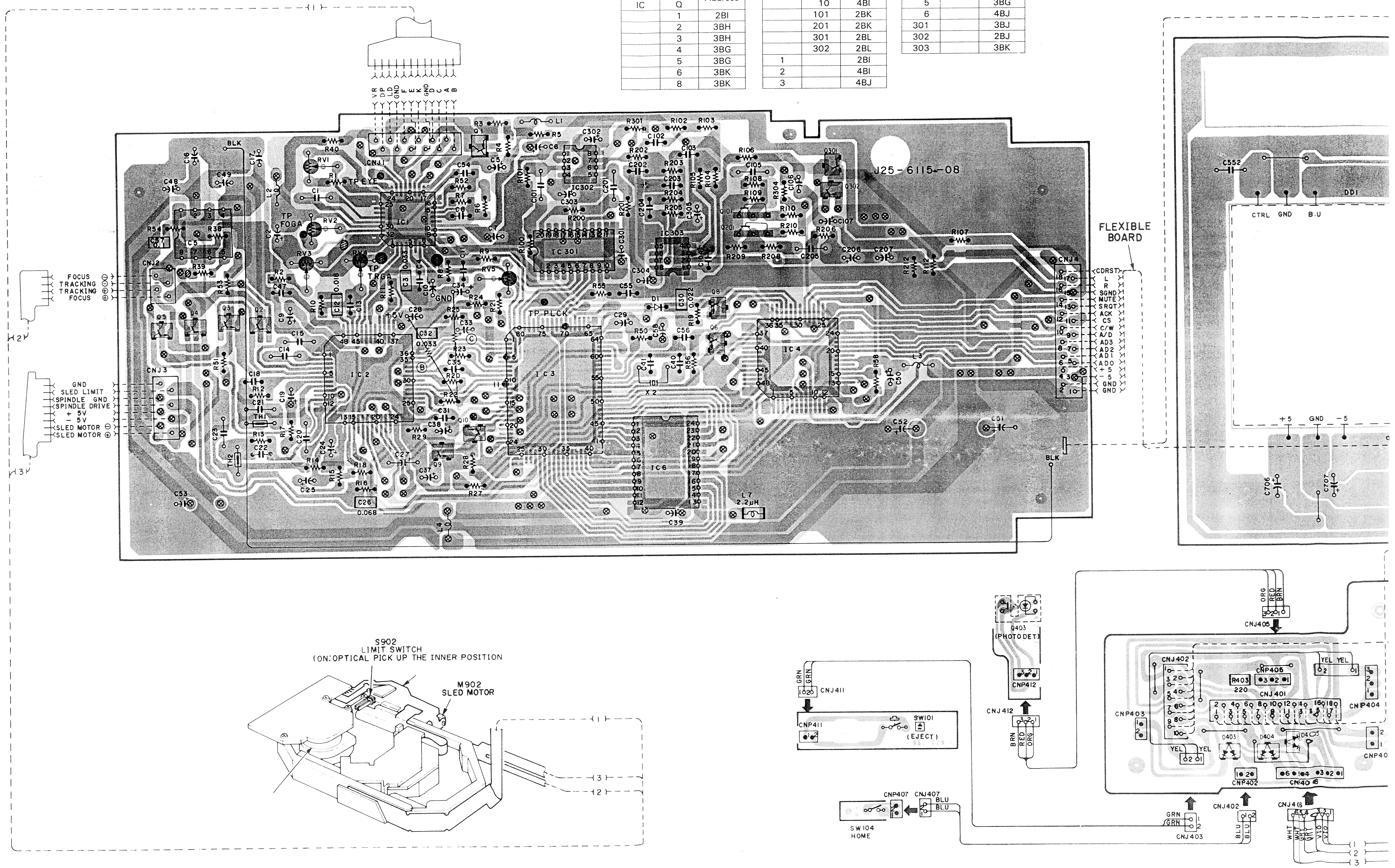
KDC-C100 (K) 2/2

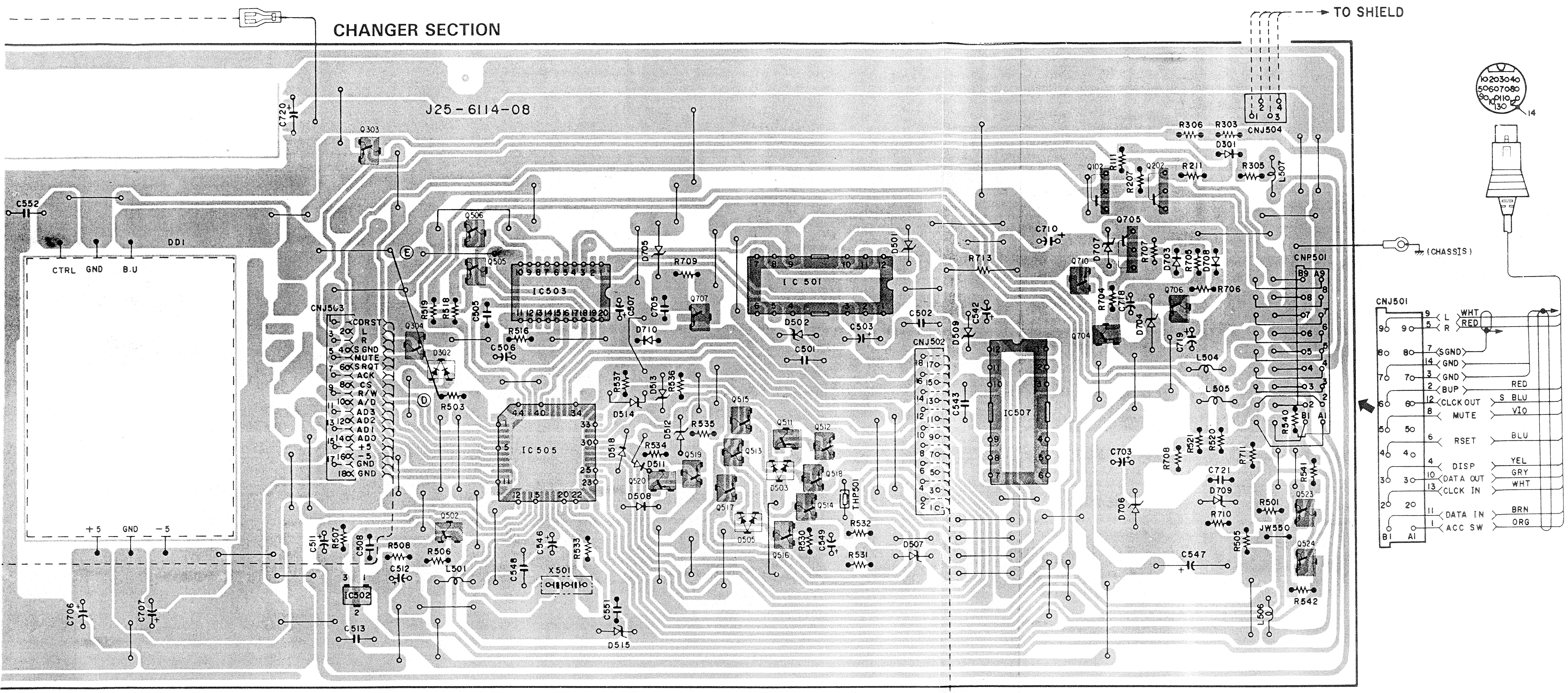
Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (Foil side view)

CHANGER SECTION-1

Ref. No. IC	Ref. No. Q	Address
	1	2BI
	2	3BH
	3	3BH
	4	3BG
	5	3BG
	6	3BK
	8	3BK
	9	4BI
	10	4BI
	101	2BK
	201	2BK
	301	2BL
	302	2BL
1		2BI
2		4BI
3		4BJ
4		3BK
5		3BG
6		4BJ
301		3BJ
302		2BJ
303		3BK

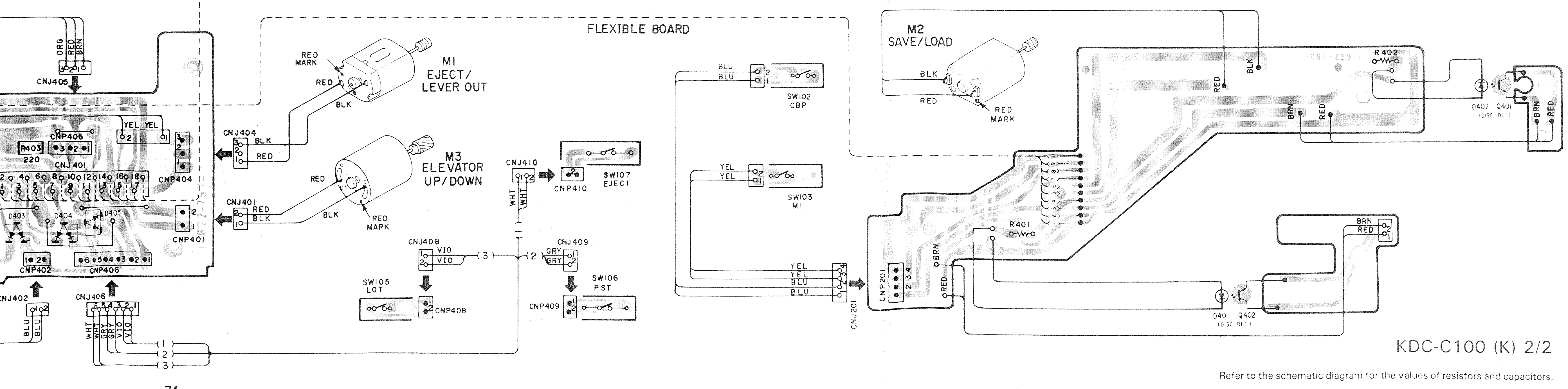

VR
DP
LD
GND
F
E
K
GND
D
C
A
B
CNJ1
BLK
J25-6115-08
FOCUS ⊖
TRACKING ⊖
TRACKING ⊕
FOCUS ⊕
GND
SLED LIMIT
SPINDLE GND
SPINDLE DRIVE
+ 5V
− 5V
SLED MOTOR ⊖
SLED MOTOR ⊕
CNJ2
CNJ3
CNJ4
IC1
IC2
IC3
IC4
IC5
IC6
IC301
IC302
IC303
TP EYE
TP FOGA
TP TRGA
TP PLCK
RV1
RV2
RV3
RV4
RV5
X2
L7 2.2μH
FLEXIBLE BOARD
CDRST
L
R
SGND
MUTE
SRQT
ACK
CS
C/W
A/D
AD3
AD2
AD1
ADO
+5
−5
GND
GND
CTRL
GND
B.U
DDI
+5
GND
−5
C552
C706
C707
S902
LIMIT SWITCH
(ON:OPTICAL PICK UP THE INNER POSITION
M902
SLED MOTOR
Q403
(PHOTO DET)
CNP412
CNJ412
CNJ411
CNP411
SW101
(EJECT)
CNP407
CNJ407
SW104
HOME
CNJ405
CNJ402
CNP402
CNP403
CNP404
CNP405
CNJ401
CNJ403
CNJ406
R403 220
D403
D404
D405
GRN
BLU
BRN
RED
ORG
YEL
WHT
VIO


CHANGER SECTION
TO SHIELD
J25-6114-08
CNJ503
CNJ502
CNJ504
CNP501
CNJ501
IC501
IC502
IC503
IC505
IC507
DDI
CTRL
GND
B.U
+5
GND
-5
CDRST
MUTE
SRQT
ACK
CS
R/W
A/D
AD3
AD2
AD1
AD0
(CHASSIS)
X501
JW550
WHT
RED
BLU
S BLU
VIO
YEL
GRY
BRN
ORG
SGND
BUP
CLCK OUT
RSET
DISP
DATA OUT
CLCK IN
DATA IN
ACC SW

1	ACC SW
2	B.UP
3	GND
4	DISP
5	R
6	RSET
7	S GND
8	MUTE
9	L
10	DATA OUT
11	DATA IN
12	CLCK OUT
13	CLCK IN
14	GND

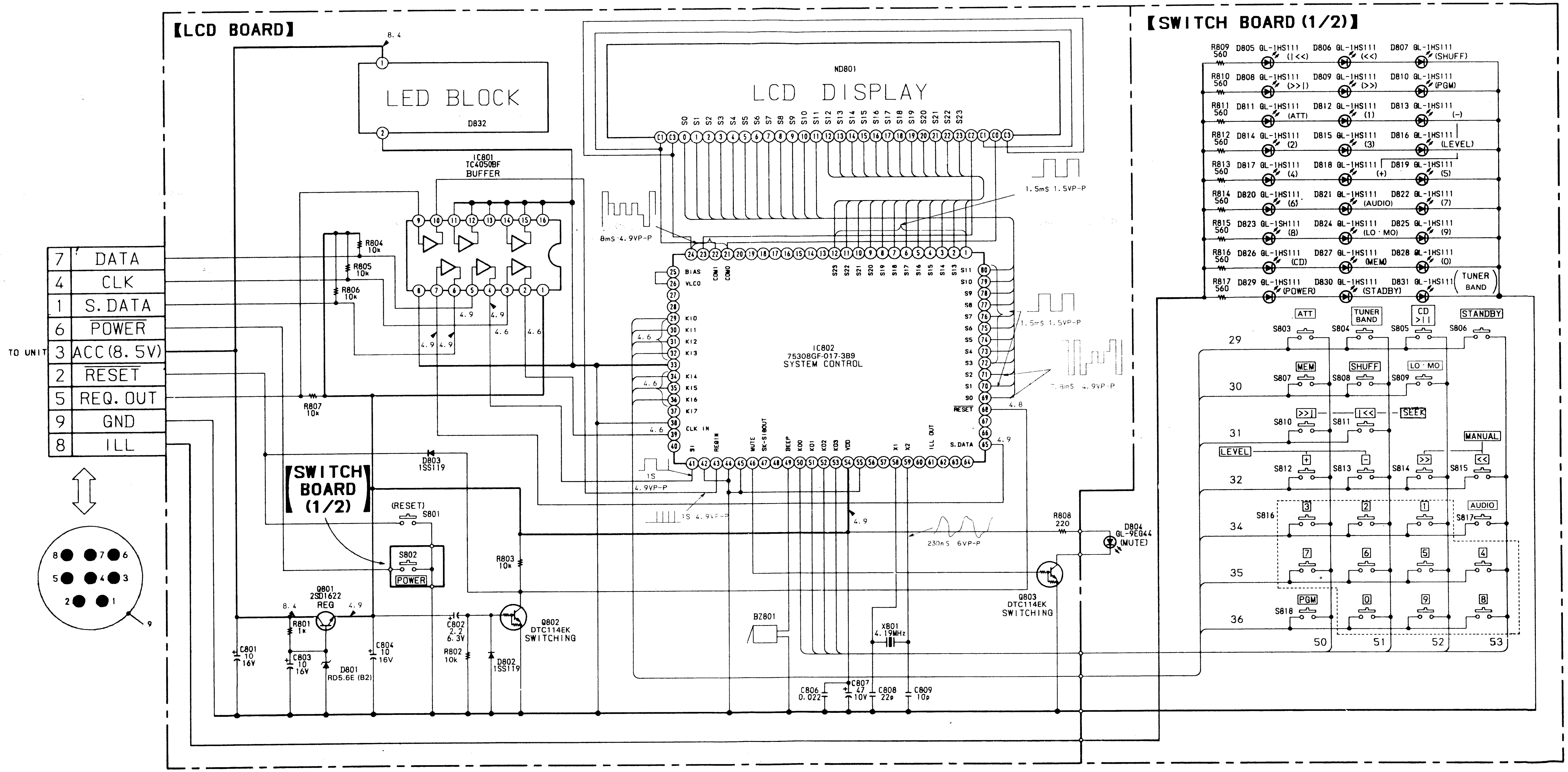
CHANGER SECTION-2

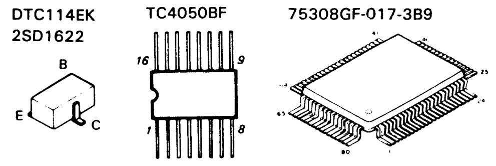
Ref. No.		Address
IC	Q	
	102	2BT
	202	2BT
	303	2BP
	304	3BP
	502	4BQ
	505	2BQ
	506	2BQ
	511	3BR
	512	3BS
	513	3BR
	514	4BS
	515	3BR
	516	4BS
	517	4BR
	518	4BS
	519	4BR
	520	4BR
	523	4BU
	524	4BU
	704	3BT
	705	2BT
	706	3BU
	707	3BU
	710	3BT
501		2BS
502		4BP
503		3BQ
505		3BQ
507		2BT


FLEXIBLE BOARD
M1
EJECT/
LEVER OUT
M2
SAVE/LOAD
M3
ELEVATOR
UP/DOWN
RED MARK
RED
BLK
CNJ404
CNJ401
CNJ405
CNJ402
CNJ406
CNJ408
CNJ409
CNJ410
CNP401
CNP402
CNP404
CNP405
CNP406
CNP408
CNP409
CNP410
CNP201
CNJ201
R403
220
R401
R402
D401
D402
D403
D404
D405
Q401
Q402
(DISC DET)
SW102
CBP
SW103
MI
SW105
LOT
SW106
PST
SW107
EJECT
YEL
BLU
WHT
GRY
VIO
ORG
BRN

KDC-C100 (K) 2/2

Refer to the schematic diagram for the values of resistors and capacitors.


【LCD BOARD】
【SWITCH BOARD (1/2)】
LED BLOCK
D832
LCD DISPLAY
ND801
IC801
TC4050BF
BUFFER
IC802
75308GF-017-3B9
SYSTEM CONTROL
7 DATA
4 CLK
1 S.DATA
6 POWER
3 ACC(8.5V)
2 RESET
5 REQ.OUT
9 GND
8 ILL
TO UNIT
SWITCH BOARD (1/2)
(RESET) S801
S802 POWER
Q801 2SD1622 REG
Q802 DTC114EK SWITCHING
Q803 DTC114EK SWITCHING
D801 RD5.6E (B2)
D802 1SS119
D803 1SS119
D804 GL-9E044 (MUTE)
BZ801
X801 4.19MHz
R801 1k
R802 10k
R803 10k
R804 10k
R805 10k
R806 10k
R807 10k
R808 220
C801 10 16V
C802 2.2 6.3V
C803 10 16V
C804 10 16V
C806 0.022
C807 47 10V
C808 22p
C809 10p
8mS 4.9VP-P
1.5mS 1.5VP-P
230nS 6VP-P
1S 4.9VP-P
ATT
TUNER BAND
CD >||
STANDBY
MEM
SHUFF
LO·MO
SEEK
MANUAL
LEVEL
AUDIO
PGM
S803
S804
S805
S806
S807
S808
S809
S810
S811
S812
S813
S814
S815
S816
S817
S818
R809 560
R810 560
R811 560
R812 560
R813 560
R814 560
R815 560
R816 560
R817 560
GL-1HS111


DTC114EK
2SD1622
B
E
C
TC4050BF
16
9
1
8
75308GF-017-3B9

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

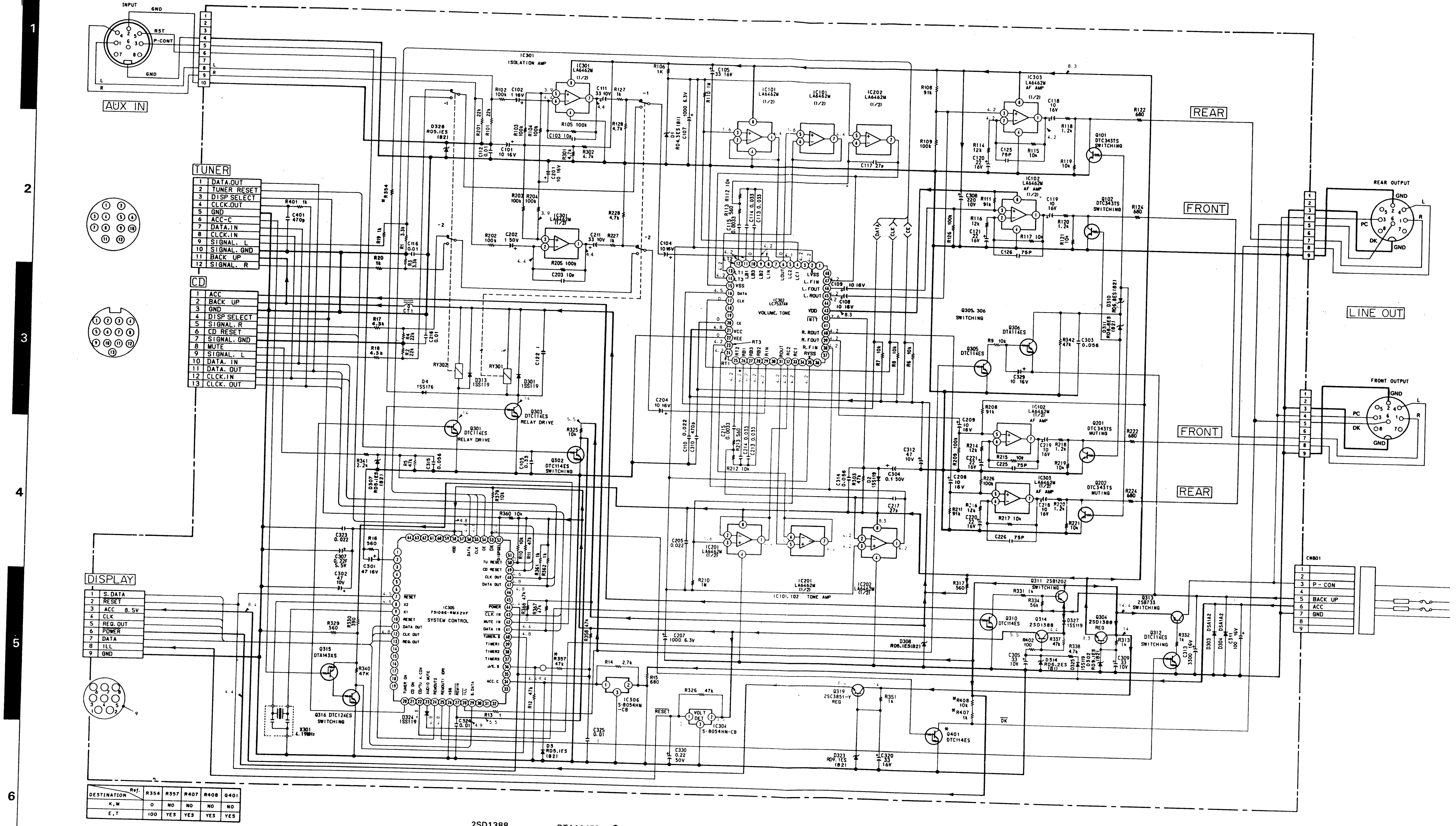
Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

CONTROLLER

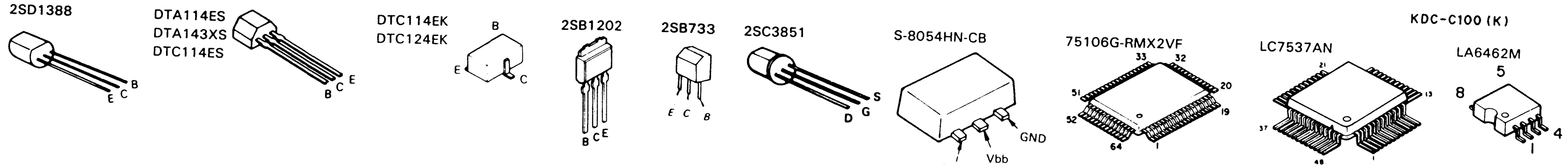
KDC-C100

KENWOOD

Y22-1440-11


J
K
L
M
N
O
P
Q
R
1
2
3
4
5
6
7
INPUT
GND
RST
P-CONT
L
R
AUX IN
TUNER
1 DATA.OUT
2 TUNER RESET
3 DISP SELECT
4 CLCK.OUT
5 GND
6 ACC-C
7 DATA.IN
8 CLCK.IN
9 SIGNAL. L
10 SIGNAL. GND
11 BACK UP
12 SIGNAL. R
CD
1 ACC
2 BACK UP
3 GND
4 DISP SELECT
5 SIGNAL. R
6 CD RESET
7 SIGNAL. GND
8 MUTE
9 SIGNAL. L
10 DATA. IN
11 DATA. OUT
12 CLCK.IN
13 CLCK. OUT
DISPLAY
1 S. DATA
2 RESET
3 ACC 8.5V
4 CLK
5 REQ. OUT
6 POWER
7 DATA
8 ILL
9 GND
IC301 ISOLATION AMP
IC301 LA6462M (1/2)
IC101 LA6462M (1/2)
IC202 LA6462M (1/2)
IC302 LC7537AN VOLUME, TONE
IC303 LA6462M AF AMP
IC102 LA6462M AF AMP
IC503 LA6462M AF AMP
IC201 LA6462M (1/2)
IC101, 102 TONE AMP
IC305 75106G-RMX2VF SYSTEM CONTROL
IC306 S-8054HN-CB
IC304 S-8054HN-CB
Q301 DTC114ES RELAY DRIVE
Q303 DTC114ES RELAY DRIVE
Q302 DTC114ES SWITCHING
Q305, 306 SWITCHING
Q101 DTC343TS SWITCHING
Q102 DTC343TS SWITCHING
Q201 DTC343TS MUTING
Q202 DTC343TS MUTING
Q311 2SB1202 SWITCHING
Q313 2SB733 SWITCHING
Q304 2SD1388 REG
Q312 DTC114ES SWITCHING
Q310 DTC114ES
Q314 2SD1388
Q315 DTA143XS
Q316 DTC124ES SWITCHING
Q319 2SC3851-Y REG
Q401 DTC114ES
X301 4.19MHz
REAR
FRONT
LINE OUT
REAR OUTPUT
FRONT OUTPUT
CN801
P-CON
BACK UP
ACC
GND
DK
PC

DESTINATION \ Ref.	R354	R357	R407	R408	Q401
K, M	0	NO	NO	NO	NO
E, T	100	YES	YES	YES	YES


2SD1388
E C B
DTA114ES
DTA143XS
DTC114ES
B C E
DTC114EK
DTC124EK
B
E
C
2SB1202
B C E
2SB733
E C B
2SC3851
D G S
S-8054HN-CB
OUT
Vbb
GND
75106G-RMX2VF
33
32
51
20
52
19
64
1
LC7537AN
37
13
48
1
KDC-C100 (K)
LA6462M
5
8
1
4

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

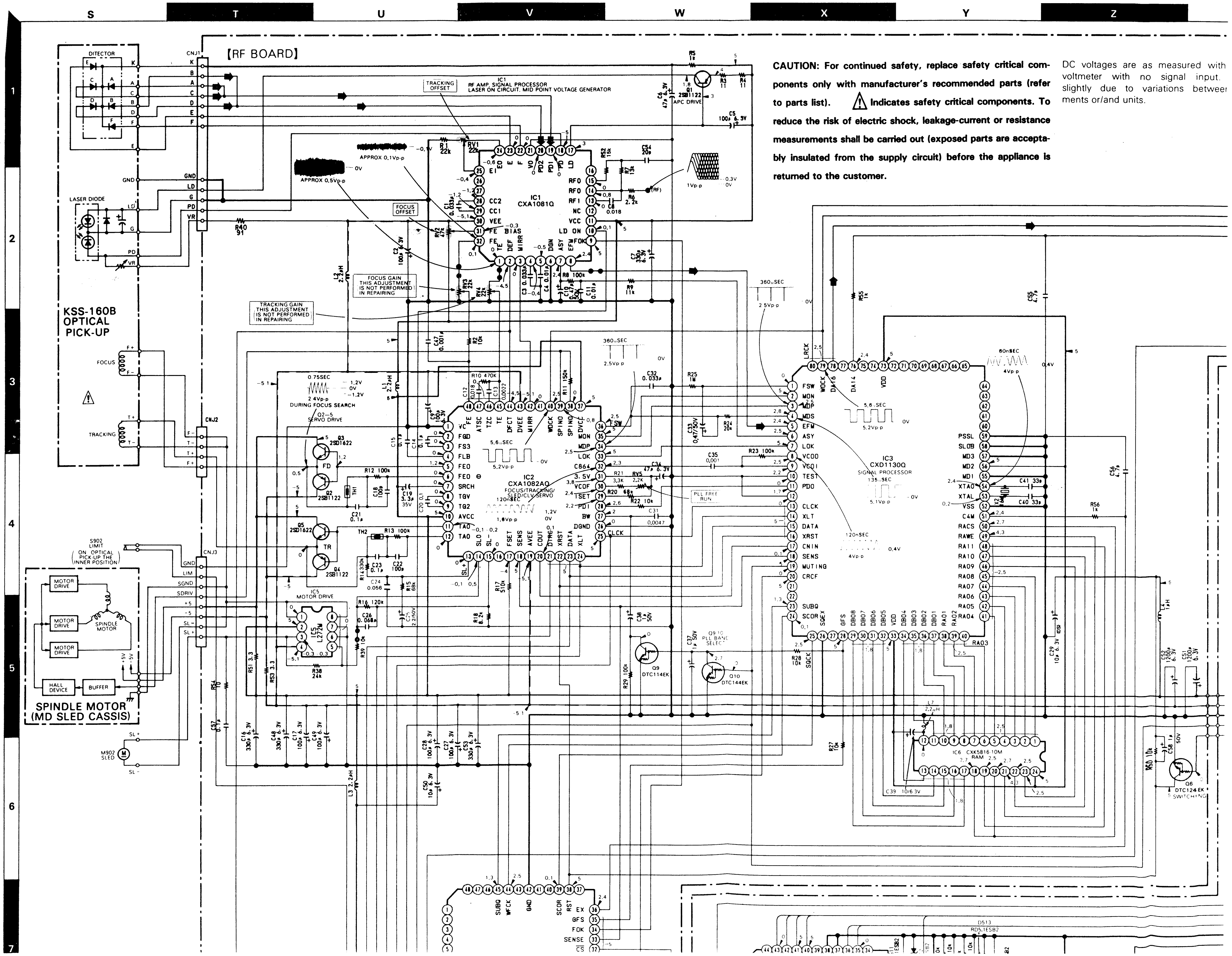
Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten geringfügig.

HIDE-AWAY

KDC-C100

KENWOOD

Y22-1440-11

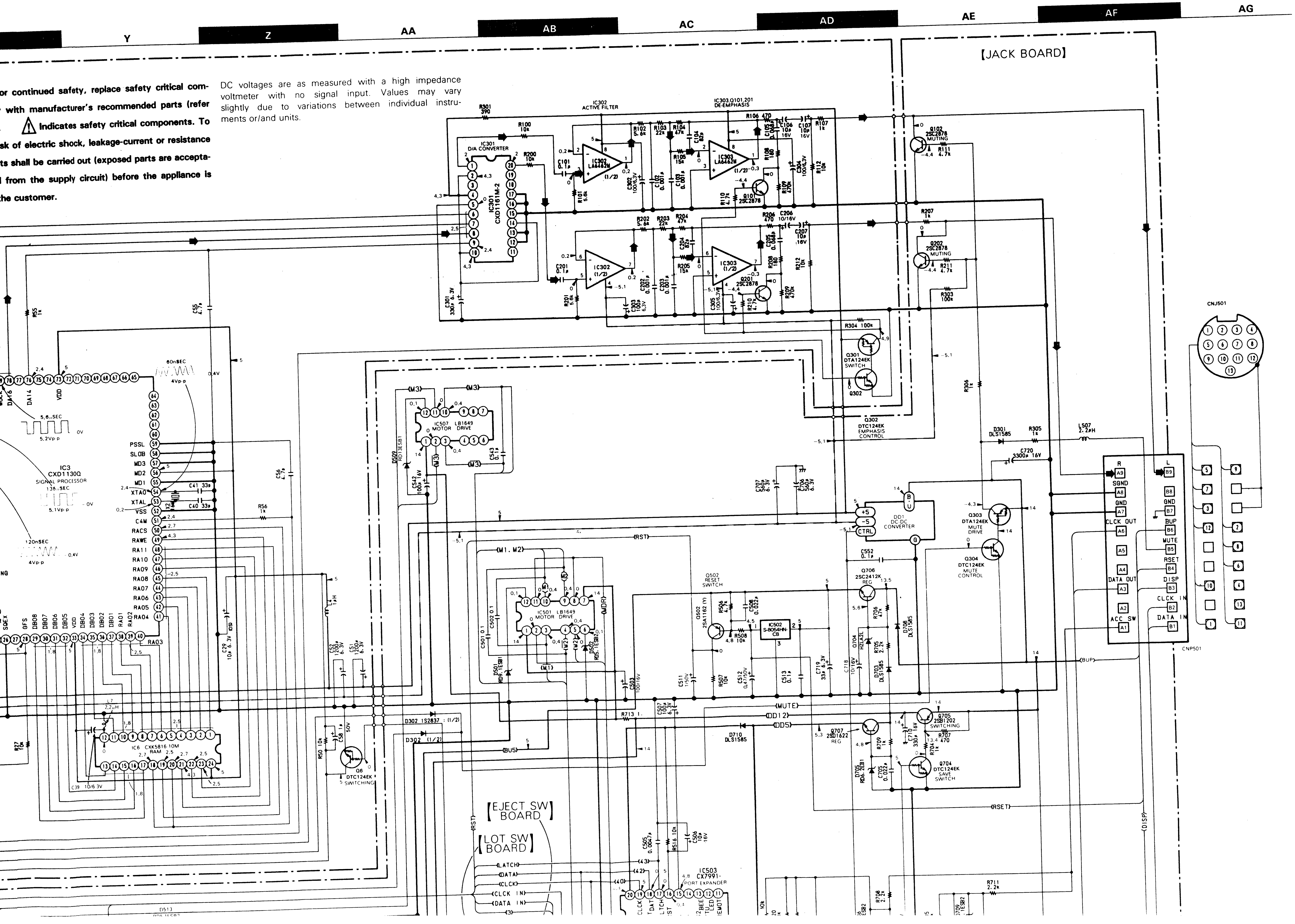

S
T
U
V
W
X
Y
Z
1
2
3
4
5
6
7
[RF BOARD]
DITECTOR
LASER DIODE
KSS-160B OPTICAL PICK-UP
FOCUS
TRACKING
CNJ1
CNJ2
CNJ3
S902 LIMIT (ON OPTICAL PICK-UP THE INNER POSITION)
MOTOR DRIVE
SPINDLE MOTOR
HALL DEVICE
BUFFER
SPINDLE MOTOR (MD SLED CASSIS)
M902 SLED
TRACKING OFFSET
IC1 RF AMP, SIGNAL PROCESSOR LASER ON CIRCUIT, MID POINT VOLTAGE GENERATOR
IC1 CXA1081Q
FOCUS OFFSET
FOCUS GAIN THIS ADJUSTMENT IS NOT PERFORMED IN REPAIRING
TRACKING GAIN THIS ADJUSTMENT IS NOT PERFORMED IN REPAIRING
APPROX 0.5Vp-p
APPROX 0.1Vp-p
Q1 2SB1122 APC DRIVE
IC2 CXA1082AQ FOCUS/TRACKING/SLED/CLV SERVO
0.75SEC
DURING FOCUS SEARCH
Q2-5 SERVO DRIVE
Q3 2SD1622
Q2 2SB1122
Q5 2SD1622
Q4 2SB1122
FD
TR
IC5 L272M MOTOR DRIVE
IC3 CXD1130Q SIGNAL PROCESSOR
PLL FREE RUN
Q9 DTC114EK
Q9,10 PLL BAND SELECT
Q10 DTC144EK
IC6 CXK5816-10M RAM
Q6 DTC124EK SWITCHING
D513 RD5.1ESB2

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DC voltages are as measured with
voltmeter with no signal input.
slightly due to variations between
ments or/and units.

or continued safety, replace safety critical com- with manufacturer's recommended parts (refer ⚠ Indicates safety critical components. To sk of electric shock, leakage-current or resistance ts shall be carried out (exposed parts are accepta- from the supply circuit) before the appliance is the customer.

DC voltages are as measured with a high impedance voltmeter with no signal input. Values may vary slightly due to variations between individual instruments or/and units.



Y
Z
AA
AB
AC
AD
AE
AF
AG
[JACK BOARD]
IC301 D/A CONVERTER
IC301 CXD1161M-2
IC302 ACTIVE FILTER
IC302 LA6462M (1/2)
IC303,Q101,201 DE-EMPHASIS
IC303 LA6462M (1/2)
Q101 2SC2878
Q201 2SC2878
Q102 2SC2878 MUTING
Q202 2SC2878 MUTING
Q301 DTA124EK SWITCH
Q302 DTC124EK EMPHASIS CONTROL
R304 100k
R303 100k
R301 390
R100 10k
R200 10k
R102 5.6k
R103 22k
R104 47k
R105 15k
R106 470
R107 1k
R108 180
R109 470k
R110 4.7k
R111 4.7k
R112 10k
R202 5.6k
R203 22k
R204 47k
R205 15k
R206 470
R207 1k
R208 180
R209 470k
R210 4.7k
R211 4.7k
R212 10k
C101 0.1µ
C201 0.1µ
C301 330µ 6.3V
C302 100/6.3V
C303 100µ 6.3V
C206 10/16V
C720 3300µ 16V
L507 2.2µH
D301 DLS1585
R305 1k
R306 1k
CNJ501
CNP501
IC3 CXD1130Q SIGNAL PROCESSOR
60nSEC 4Vp-p
5.6µSEC 5.2Vp-p
136nSEC 5.1Vp-p
120nSEC 4Vp-p
PSSL
SLOB
MD3
MD2
MD1
XTAO
XTAL
VSS
C4M
RACS
RAWE
RA11
RA10
RA09
RA08
RA07
RA06
RA05
RA04
RA03
RA02
RA01
DB01
DB02
DB03
VDD
DB05
DB06
DB07
DB08
DFS
SDEX
DA14
DA16
C41 33p
C40 33p
R56 1k
R55 1k
C55 4.7µ
C56 4.7µ
C29 10µ 6.3V
C52 1200µ 6.3V
C51 1200µ 6.3V
L7 2.2µH
IC6 CXK5816 10M RAM
C39 10/6.3V
R27 10k
R50 10k
C58 1µ 50V
Q6 DTC124EK SWITCHING
D302 1S2837 (1/2)
IC507 LB1649 MOTOR DRIVE
IC501 LB1649 MOTOR DRIVE
D509 RD13ESB1
D501 RD9.1ESB1
D502 RD5.1ESB1
C542 100µ 16V
C543 0.1µ
C501 0.1
C502 0.1
C509 100/16V
(M1.M2)
(M1)
(M2)
(M3)
(MDR)
(RST)
(BUS)
(MUTE)
(DD12)
(DD5)
(RSET)
(BUP)
(DISP)
DD1 DC-DC CONVERTER
+5
-5
CTRL
C707 560µ 6.3V
C706 560µ 6.3V
Q303 DTA124EK MUTE DRIVE
Q304 DTC124EK MUTE CONTROL
C552 0.1µ
Q502 2SA1162 (Y) RESET SWITCH
IC502 S-8054HN-CB
R504 47k
R508 10k
R507 10k
C508 0.022µ
C511 1/50V
C512 0.47/50V
C513 0.1µ
Q706 2SC2412K REG
R706 47k
Q704 HZ4A2L
R705 2.2k
D703 DLS1585
D708 DLS1585
C719 33µ 6.3V
C718 10/16V
Q707 2SD1622 REG
R709 1k
D705 RD5.1ESB1
C705 0.022µ
C710 330µ 16V
Q705 2SB1202 SWITCHING
R707 470
R704 1k
Q704 DTC124EK SAVE SWITCH
D710 DLS1585
R713 1
C507 100µ 6.3V
[EJECT SW BOARD]
[LOT SW BOARD]
(LATCH)
(DATA)
(CLCK)
(CLCK IN)
(DATA IN)
(43)
(42)
(41)
(40)
C505 0.0047µ
R516 10k
C506 10µ 16V
IC503 CX7991- PORT EXPANDER
R711 2.2k
R708 2.2k
D513
R
L
SGND
GND
CLCK OUT
DATA OUT
ACC SW
BUP
MUTE
RSET
DISP
CLCK IN
DATA IN
A1
A2
A3
A4
A5
A6
A7
A8
A9
B1
B2
B3
B4
B5
B6
B7
B8
B9

6

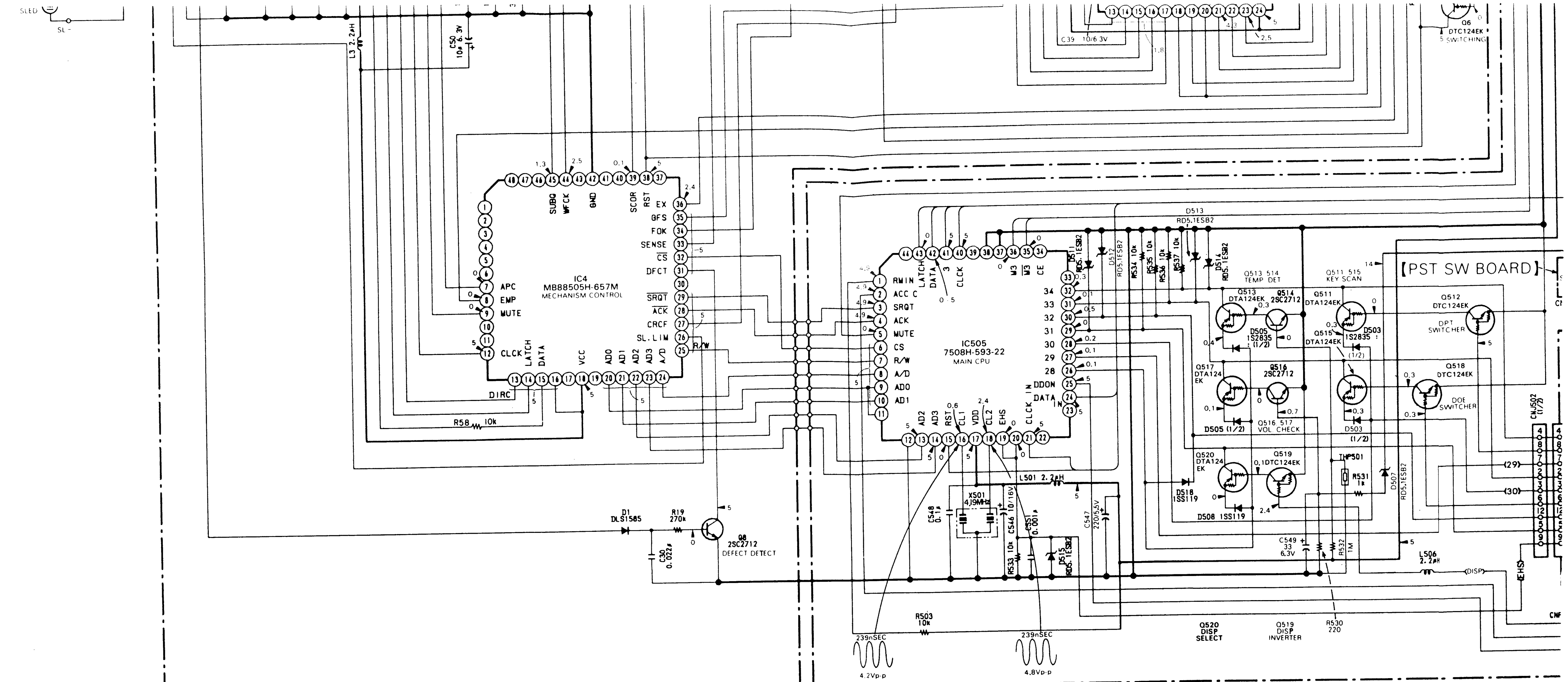
7

8

9

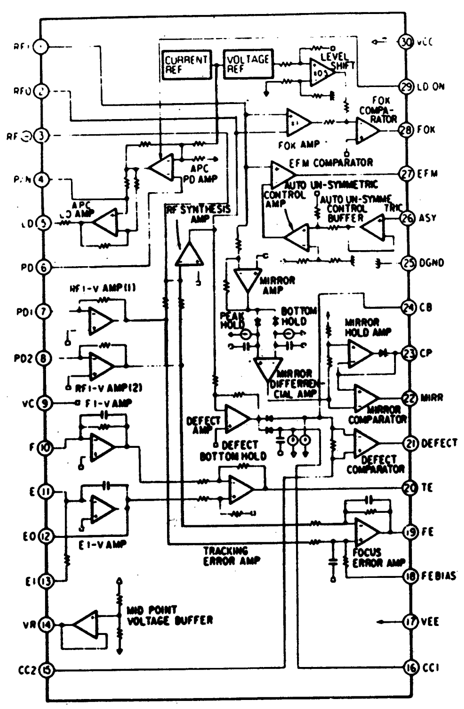
10

11

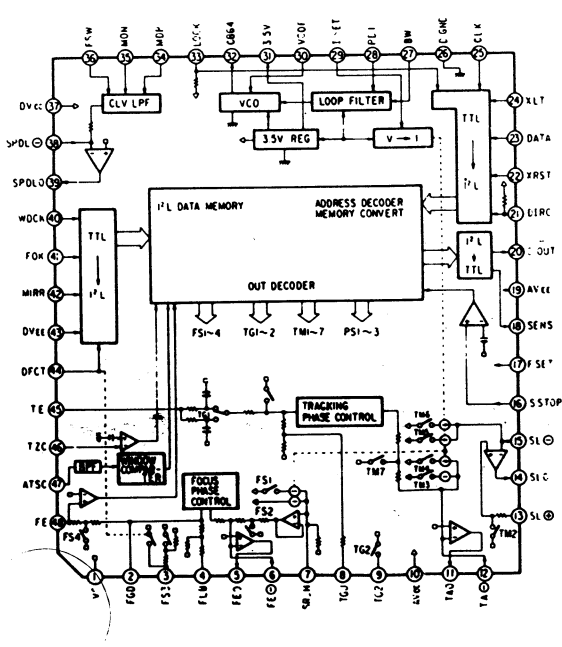

IC4
MB88505H-657M
MECHANISM CONTROL
IC505
7508H-593-22
MAIN CPU
Q8
2SC2712
DEFECT DETECT
D1
DLS1585
R19
270k
R58 10k
L3 2.2μH
C50 10μ 6.3V
C30 0.022μ
XS01
4.19MHz
L501 2.2μH
D513
RD5.1ESB2
Q513 514
TEMP DET
Q511 515
KEY SCAN
Q512
DTC124EK
DPT SWITCHER
Q518
DTC124EK
DOE SWITCHER
Q516 517
VOL CHECK
Q519
DISP INVERTER
Q520
DISP SELECT
THP501
R531
D507
RD5.1ESB2
D518
1SS119
D508 1SS119
L506 2.2μH
R503 10k
R530 220
239nSEC
4.2Vp-p
239nSEC
4.8Vp-p
Q6
DTC124EK
5 SWITCHING
C39 10/6.3V
CN502
【PST SW BOARD】
EHS
DISP

• IC BLOCK DIAGRAMS

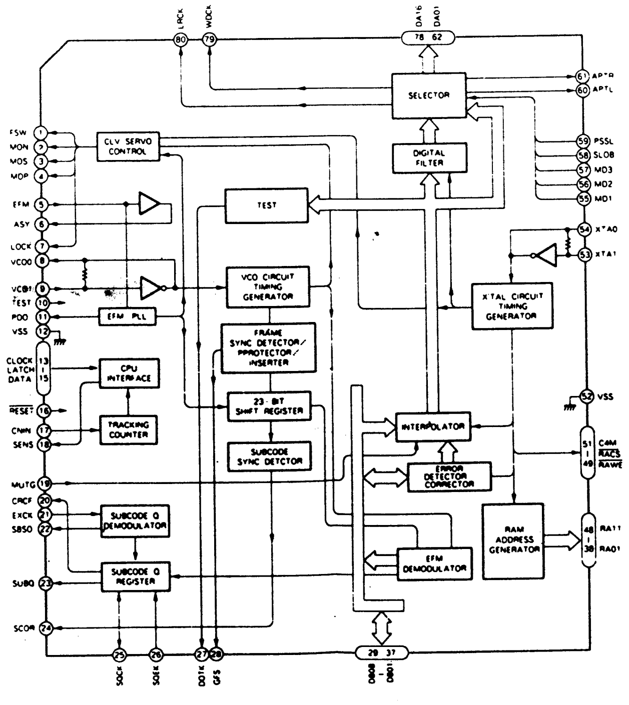
IC1 CXA1081Q


CURRENT REF
VOLTAGE REF
LEVEL SHIFT
FOK COMPARATOR
FOK AMP
EFM COMPARATOR
APC PD AMP
APC LD AMP
RF SYNTHESIS AMP
AUTO UN-SYMMETRIC CONTROL AMP
AUTO UN-SYMMETRIC CONTROL BUFFER
MIRROR AMP
PEAK HOLD
BOTTOM HOLD
MIRROR HOLD AMP
MIRROR DIFFERENTIAL AMP
MIRROR COMPARATOR
DEFECT AMP
DEFECT BOTTOM HOLD
DEFECT COMPARATOR
RF I-V AMP(1)
RF I-V AMP(2)
F I-V AMP
E I-V AMP
TRACKING ERROR AMP
FOCUS ERROR AMP
MID POINT VOLTAGE BUFFER
VCC
LD ON
FOK
EFM
ASY
DGND
CB
CP
MIRR
DEFECT
TE
FE
FEBIAS
VEE
CCI
RFI
RFO
RF
P/N
LD
PD
PD1
PD2
VC
F
E
EO
EI
VR
CC2

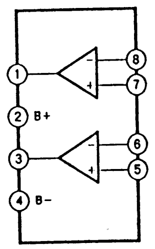
IC2 CXA1082AQ


CLV LPF
VCO
LOOP FILTER
3.5V REG
V→I
TTL
I²L
I²L DATA MEMORY
ADDRESS DECODER MEMORY CONVERT
OUT DECODER
FS1~4
TG1~2
TM1~7
PS1~3
TRACKING PHASE CONTROL
FOCUS PHASE CONTROL
XLT
DATA
XRST
DIRC
CLK
SENS
SSTOP
SL⊖
SLC
SL⊕
DVCC
SPDLO
WDCK
FOK
MIRR
DVEE
DFCT
TE
TZC
ATSC
FE

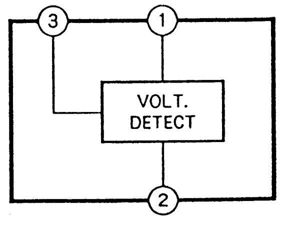
IC3 CXD1130Q

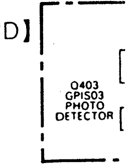

CLV SERVO CONTROL
SELECTOR
DIGITAL FILTER
TEST
VCO CIRCUIT TIMING GENERATOR
FRAME SYNC DETECTOR/ PROTECTOR/ INSERTER
23 BIT SHIFT REGISTER
SUBCODE SYNC DETECTOR
CPU INTERFACE
TRACKING COUNTER
EFM PLL
X'TAL CIRCUIT TIMING GENERATOR
INTERPOLATOR
ERROR DETECTOR CORRECTOR
EFM DEMODULATOR
RAM ADDRESS GENERATOR
SUBCODE Q DEMODULATOR
SUBCODE Q REGISTER
FSW
MON
MDS
MDP
EFM
ASY
LOCK
VCOO
VCOI
TEST
PDO
VSS
CLOCK
LATCH
DATA
RESET
CNIN
SENS
MUTG
CRCF
EXCK
SBSO
SUBQ
SCOR
XTAO
XTAI
PSSL
SLOB
MD3
MD2
MD1
VSS
C4M
RAZS
RAWE
RA11
RA01

IC5 L272M

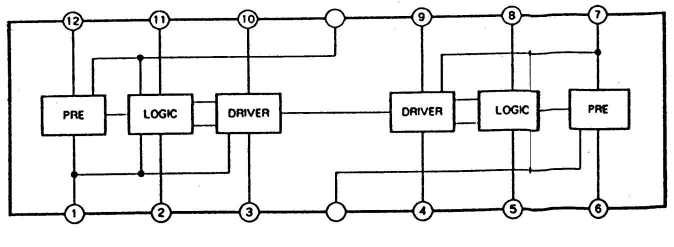


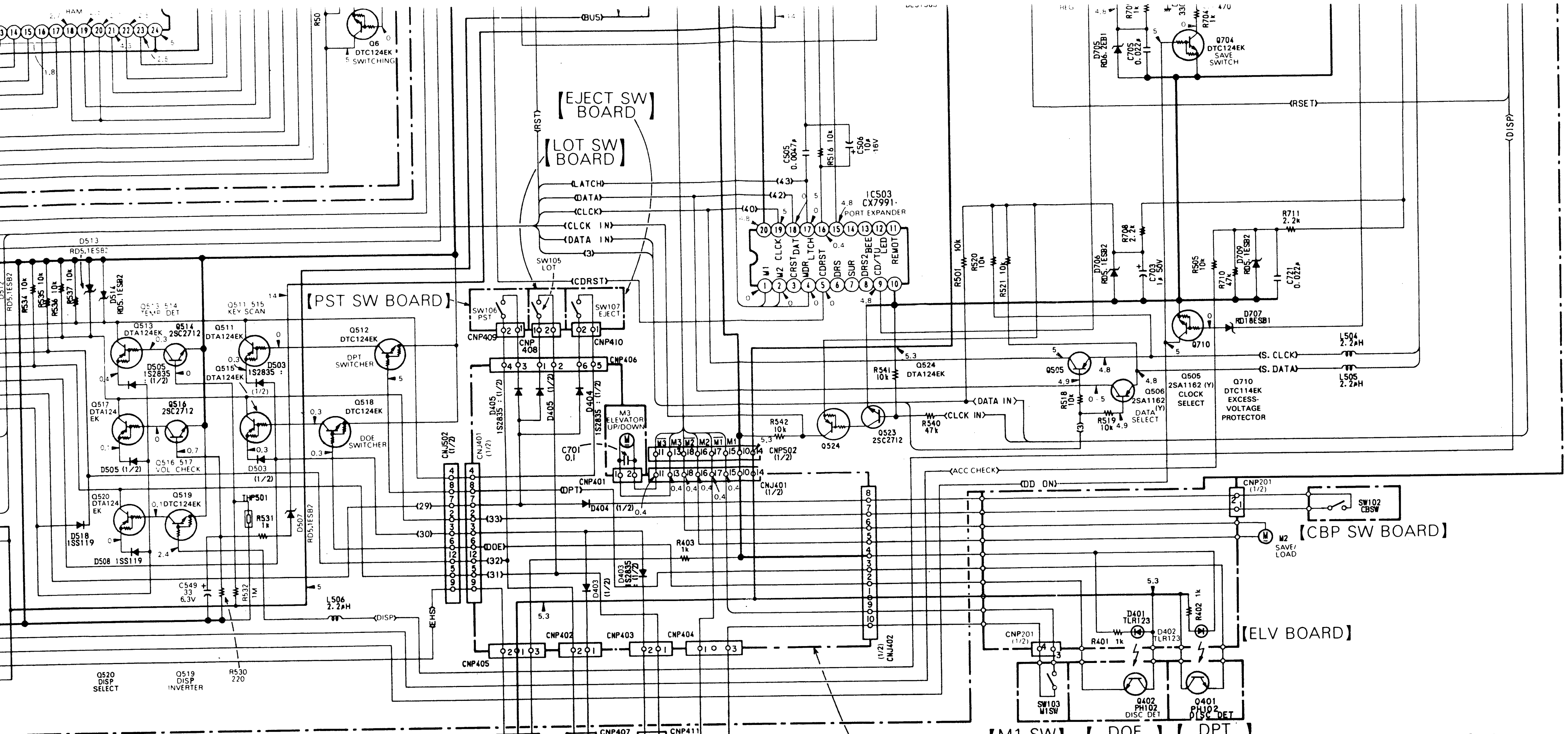
IC502 S-8054HN-CB


VOLT. DETECT

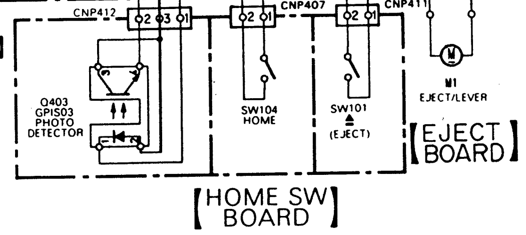

【EHS BOARD】
Q403
GP1S03
PHOTO DETECTOR

IC501, 507 LB1649


PRE
LOGIC
DRIVER
DRIVER
LOGIC
PRE



Q6 DTC124EK SWITCHING
(BUS)
(RST)
[EJECT SW BOARD]
[LOT SW BOARD]
(LATCH)
(DATA)
(CLCK)
(CLCK IN)
(DATA IN)
(CDRST)
IC503 CX7991 PORT EXPANDER
M1 M2 CLCK DATA CRST MDR LTCH CDRST DRS SUR DRS2 BEEP CD/TU LED REMOTE
C505 R516 10k C506 10μ 16V
(RSET)
(DISP)
Q704 DTC124EK SAVE SWITCH
D705 RD6.2EB1
C705 0.022μ
R711 2.2k
R708 2.2k
D706 RD5.1ESB2
C703 1μ 50V
R505 10k
R710 47k
D709 RD5.1ESB2
C721 0.022μ
D707 RD18ESB1
Q710
L504 2.2μH
L505 2.2μH
(S. CLCK)
(S. DATA)
Q710 DTC114EK EXCESS-VOLTAGE PROTECTOR
Q505 2SA1162 (Y) CLOCK SELECT
Q506 2SA1162 (Y) DATA SELECT
R501 10k
R520 10k
R521 10k
R518 10k
R519 10k
Q524 DTA124EK
R541 10k
R542 10k
R540 47k
Q523 2SC2712
(DATA IN)
(CLCK IN)
[PST SW BOARD]
SW106 PST
SW105 LOT
SW107 EJECT
CNP409
CNP408
CNP410
CNP406
D405 1S2835 (1/2)
D404 1S2835 (1/2)
M3 ELEVATOR UP/DOWN
C701 0.1
CNP502 (1/2)
CNJ401 (1/2)
M3 M3 M2 M2 M1 M1
Q512 DTC124EK DPT SWITCHER
Q518 DTC124EK DOE SWITCHER
Q513 DTA124EK
Q514 2SC2712
Q513, 514 TEMP. DET
Q511 DTA124EK
Q511, 515 KEY SCAN
D505 1S2835 (1/2)
Q515 DTA124EK
D503 1S2835
Q517 DTA124EK
Q516 2SC2712
C516, 517 VOL CHECK
Q520 DTA124EK
Q519 DTC124EK
D518 1SS119
D508 1SS119
TH501
R531 1k
D507 RD5.1ESB2
C549 33 6.3V
R532 1M
L506 2.2μH
D513 RD5.1ESB2
D514 RD5.1ESB2
R534 10k
R535 10k
R536 10k
R537 10k
Q520 DISP SELECT
Q519 DISP INVERTER
R530 220
CNP502 (1/2)
CNJ401 (1/2)
(29) (30) (33) (DOE) (32) (31) (DPT)
(EHS)
(DISP)
R403 1k
D403 1S2835 (1/2)
CNP405
CNP402
CNP403
CNP404
(ACC CHECK)
(DD ON)
CNP201 (1/2)
SW102 CBSW
[CBP SW BOARD]
M2 SAVE/LOAD
D401 TLR123
D402 TLR123
R401 1k
R402 1k
[ELV BOARD]
CNJ402 (1/2)
SW103 M1SW
Q402 PH102 DISC DET
Q401 PH102 DISC DET



CNP412
CNP407
CNP411
Q403 GP1S03 PHOTO DETECTOR
SW104 HOME
SW101 (EJECT)
M1 EJECT/LEVER
[EJECT BOARD]
[HOME SW BOARD]

[EHS BOARD]

[RELAY BOARD]

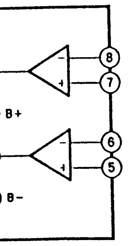
[M1 SW BOARD]

[DOE BOARD]

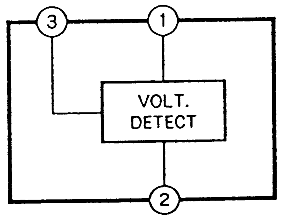
[DPT BOARD]

CHANGER

IC5 L272M

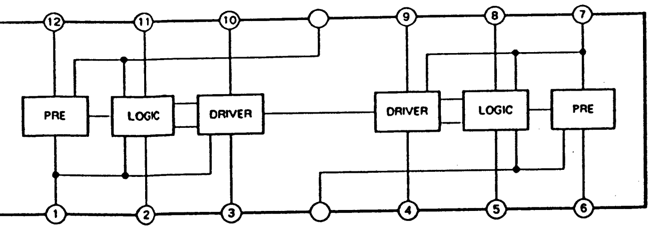


IC502 S-8054HN-CB

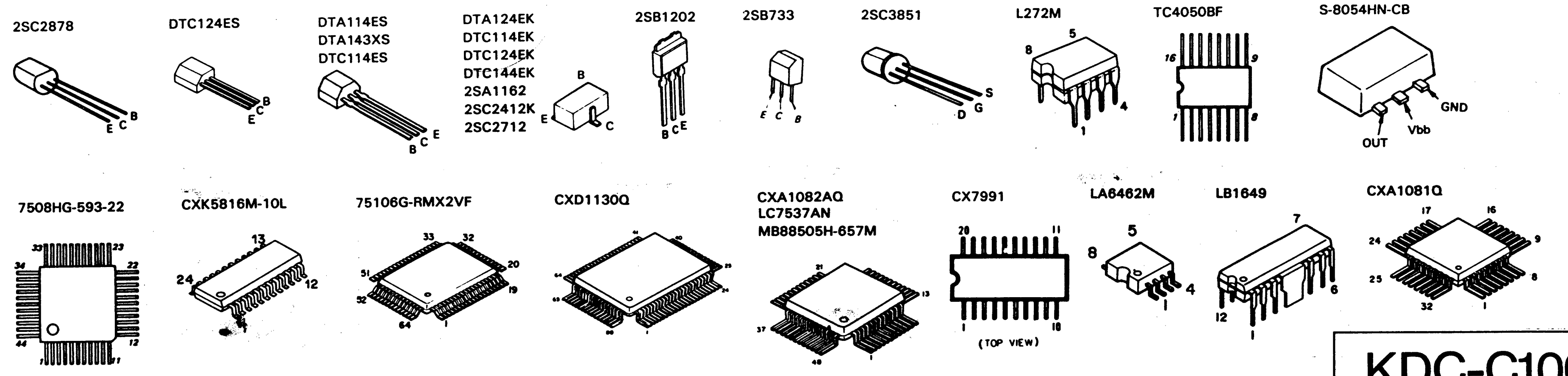


3
1
VOLT. DETECT
2

IC501, 507 LB1649



12
11
10
9
8
7
PRE
LOGIC
DRIVER
DRIVER
LOGIC
PRE
1
2
3
4
5
6



2SC2878
E C B
DTC124ES
E C B
DTA114ES
DTA143XS
DTC114ES
B C E
DTA124EK
DTC114EK
DTC124EK
DTC144EK
2SA1162
2SC2412K
2SC2712
B E C
2SB1202
B C E
2SB733
E C B
2SC3851
D G S
L272M
8 5 1 4
TC4050BF
16 9 1 8
S-8054HN-CB
GND OUT Vbb
7508HG-593-22
33 23 34 22 44 12 1 11
CXK5816M-10L
13 24 12
75106G-RMX2VF
33 32 20 51 52 64 1 19
CXD1130Q
CXA1082AQ
LC7537AN
MB88505H-657M
CX7991
20 11 1 10
(TOP VIEW)
LA6462M
5 8 4 1
LB1649
7 12 1 6
CXA1081Q
17 16 24 9 25 8 32 1

KDC-C100

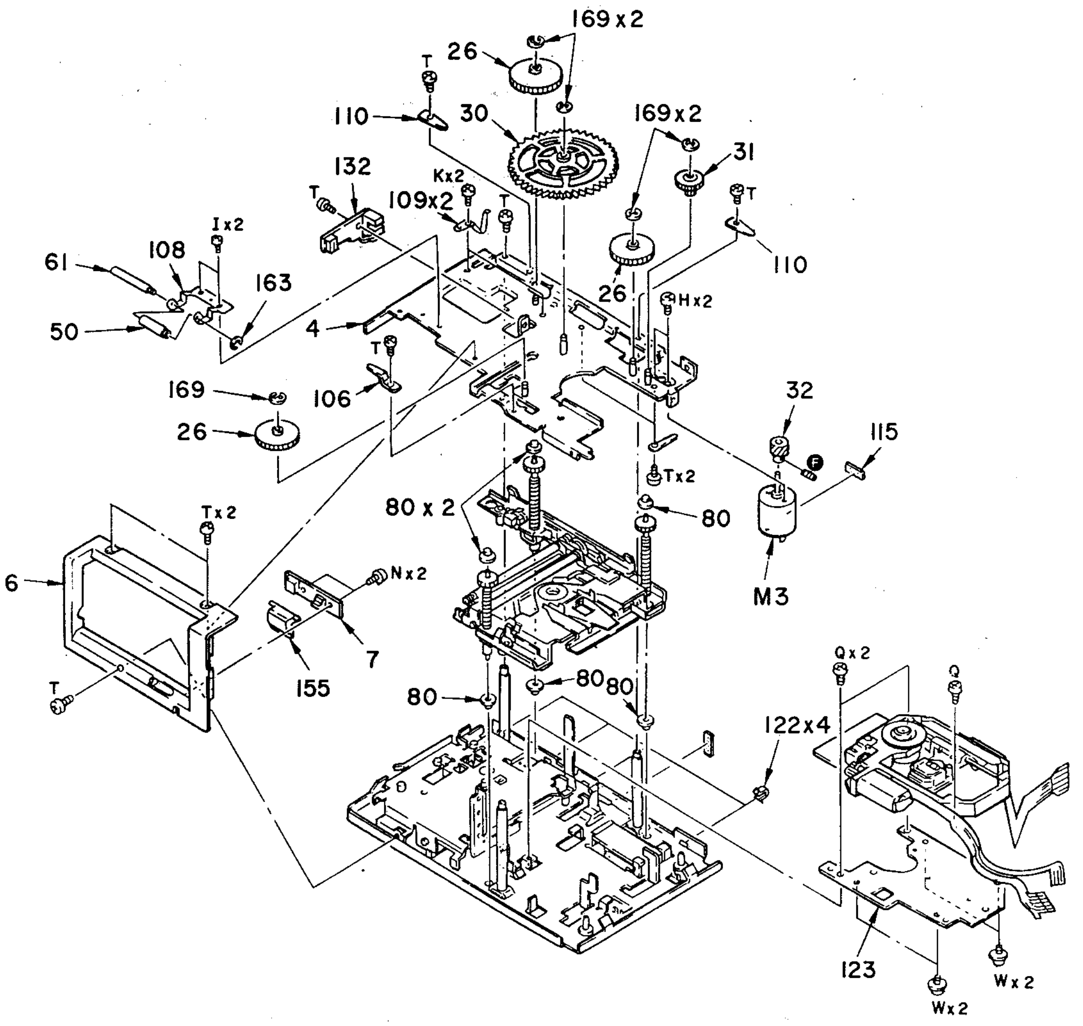
KENWOOD

Y22-1440-11

KDC-C100

EXPLODED VIEW (MECHANISM)

A
B
1
2
3

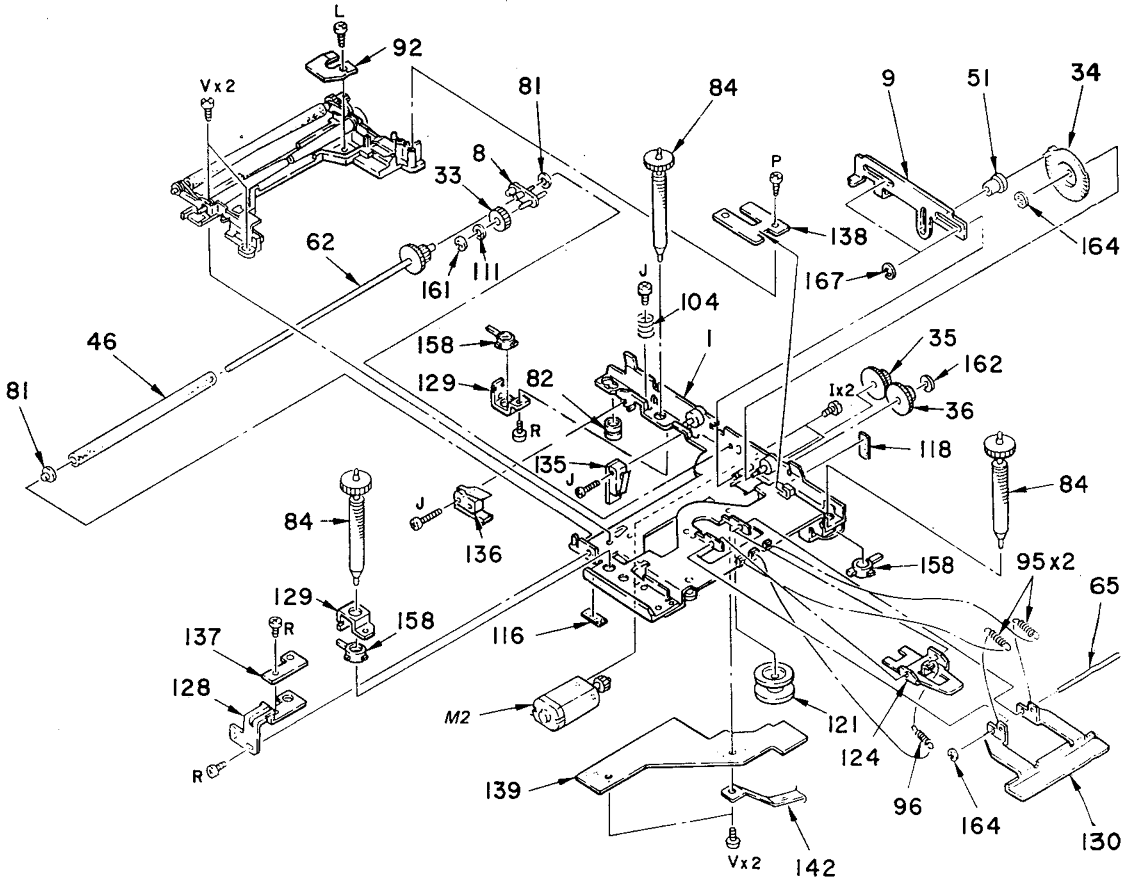

169x2
26
T
110
30
169x2
31
132
Kx2
T
109x2
T
T
Ix2
110
61
108
163
26
Hx2
50
4
T
169
106
32
115
26
F
Tx2
Tx2
80 x 2
80
6
Nx2
M3
7
T
155
Qx2
Q
80
80
80
80
122x4
123
Wx2
Wx2

F			: N09-2639-08
H	M3x3	BLK	: N30-3003-45
I	M2x3	BLK	: N30-2003-45
K	M2.6x3 (Bi)	BLK	: N35-2603-45
N	Ø2.6x5 (T)		: N52-2605-46
Q	Ø2x4 (Tap)	BLK	: N84-2004-45
T	Ø2.6x5 (Tap)	BLK	: N84-2605-45
W	M2x5 (TP)		: N90-2005-46

KDC-C100 (A/5)

Parts with the exploded numbers larger than 700 are not supplied.

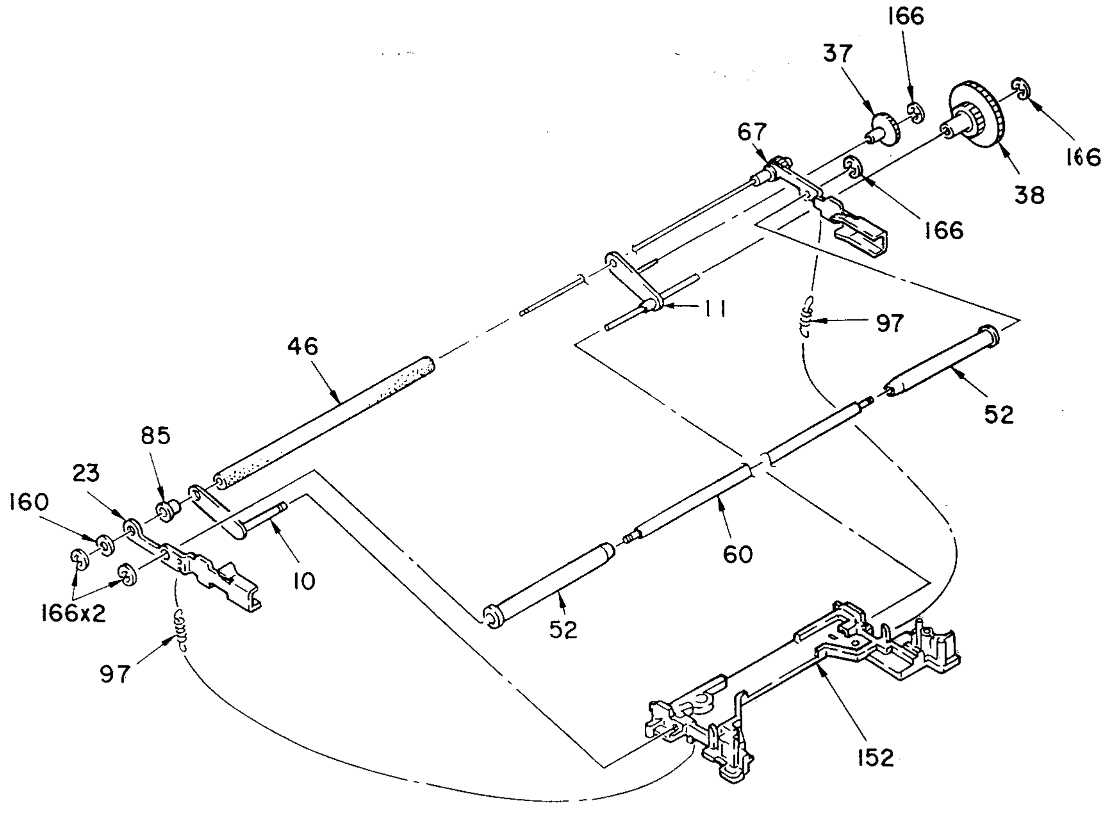
EXPLODED VIEW (MECHANISM)


L
92
Vx2
81
84
9
51
34
8
33
P
62
138
164
111
161
167
J
104
46
158
1
35
162
81
129
82
Ix2
36
R
118
135
J
84
84
J
136
158
95x2
65
129
R
158
137
116
128
M2
121
124
R
139
96
164
130
Vx2
142

I	M2x3	BLK	: N30-2003-45
J	M2x8 (Bi)	BLK	: N35-2008-45
L	M2.6x6(Bi)	BLK	: N35-2606-45
P	Ø2.6x5(T)		: N52-2605-46
R	Ø2x4 (Tap)		: N84-2004-46
V	Ø2.6x5 (Tap)		: N84-2605-46

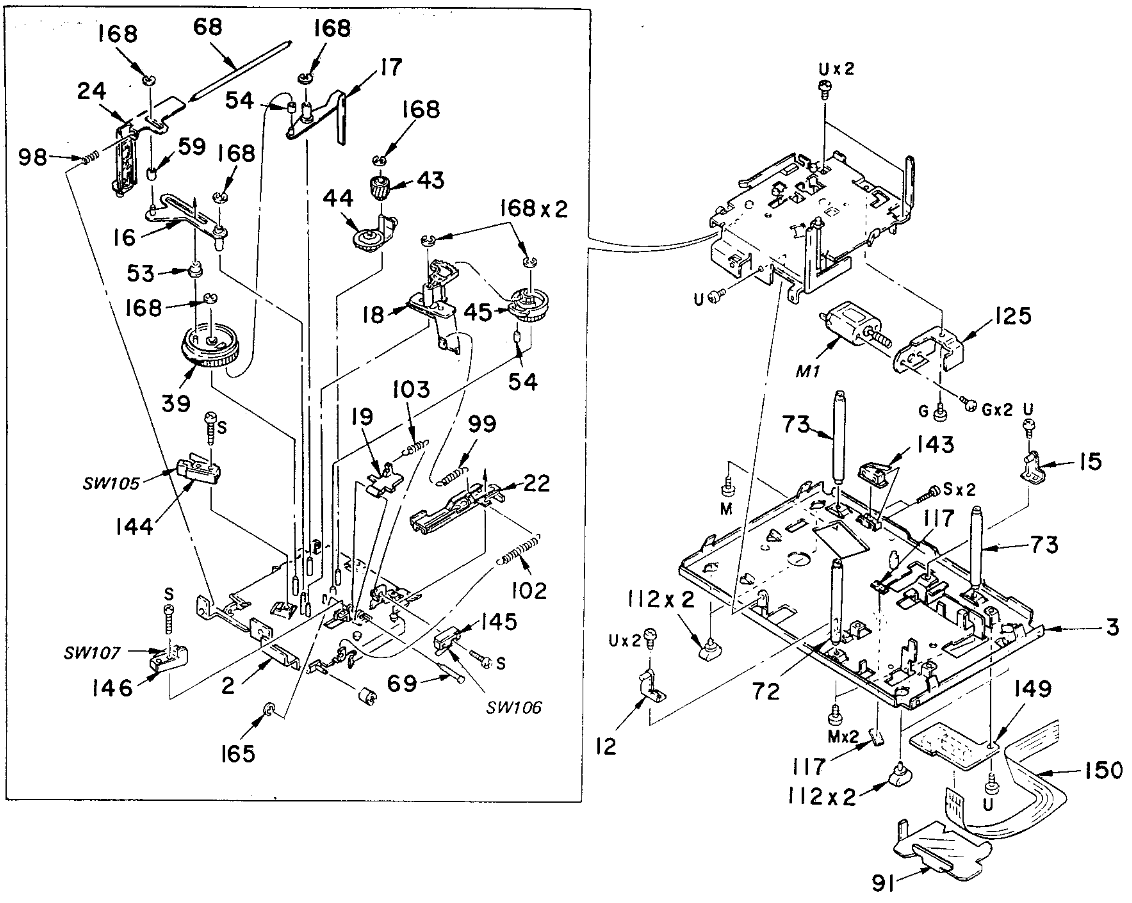
KDC-C100(B/5)

EXPLODED VIEW (MECHANISM)


E
F
1
2
3
166
37
67
166
38
166
11
97
46
52
85
23
160
10
60
166x2
52
97
152
KDC-C100(C/5)

Parts with the exploded numbers larger than 700 are not supplied.

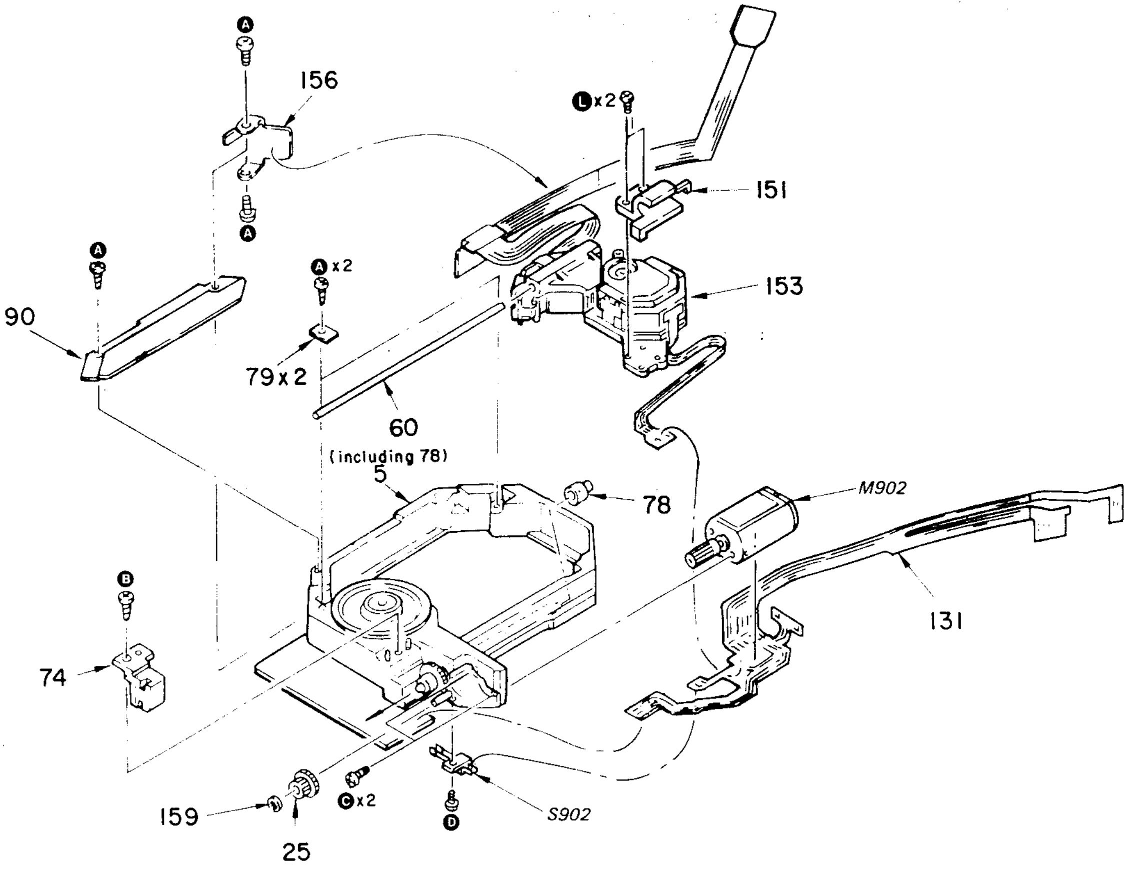
EXPLODED VIEW (MECHANISM)


168
68
168
17
24
54
168
98
59
168
43
44
168x2
16
53
168
18
45
39
54
103
19
99
S
SW105
22
144
102
S
145
SW107
146
2
69
S
SW106
165
Ux2
U
125
M1
73
G
Gx2
U
143
15
M
Sx2
117
73
112x2
3
Ux2
72
149
12
Mx2
117
150
112x2
U
91

G	M2.6x3			: N30-2603-46
M	M3x5	(Bi)	BLK	: N35-3005-45
S	ø2x10	(Tap)		: N84-2010-46
U	ø2.6x5	(Tap)	BLK	: N84-2605-45

KDC-C100(D/5)

EXPLODED VIEW (MECHANISM)


I
J
1
2
3
Ⓐ
156
Ⓛx2
151
Ⓐ
Ⓐ
Ⓐx2
153
90
79x2
60
(including 78)
5
78
M902
Ⓑ
131
74
159
Ⓒx2
Ⓓ
S902
25

Ⓐ M2x4 : N09-1304-05
Ⓑ : N09-1936-08
Ⓒ : N09-1942-08
Ⓓ : N09-1943-08
Ⓔ : N09-1944-08

KDC-C100 (E/5)

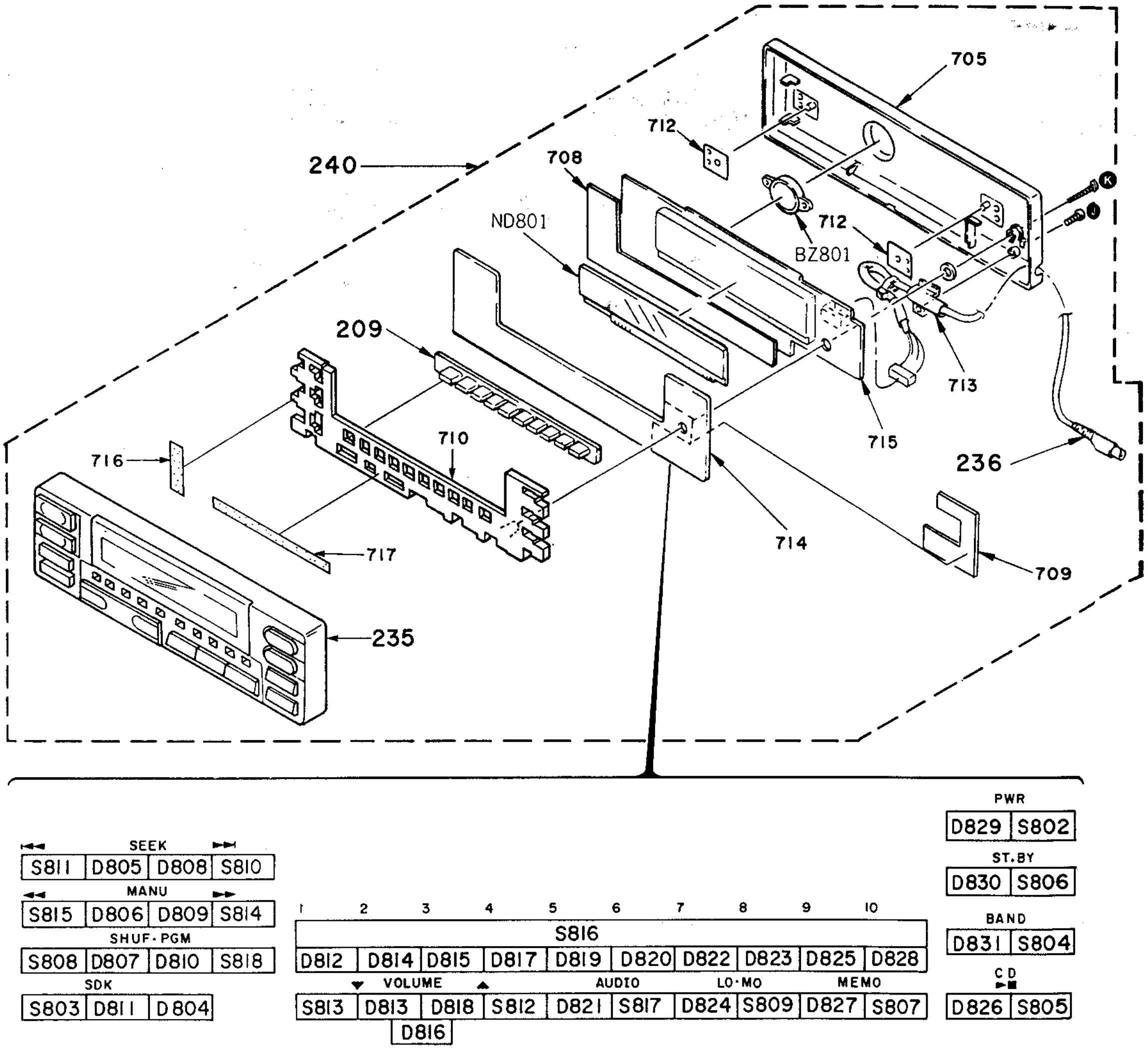
Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)

K L

1

Ⓚ : N09-2621-08
Ⓙ : N09-2622-08


705
712
708
240
ND801
712
BZ801
Ⓚ
Ⓙ
209
713
715
236
710
716
714
709
717
235
PWR
D829 S802
SEEK
S811 D805 D808 S810
ST.BY
D830 S806
MANU
S815 D806 D809 S814
1 2 3 4 5 6 7 8 9 10
S816
BAND
D831 S804
SHUF·PGM
S808 D807 D810 S818
D812 D814 D815 D817 D819 D820 D822 D823 D825 D828
SDK
▼ VOLUME ▲
AUDIO
LO·MO
MEMO
CD
S803 D811 D804
S813 D813 D818 S812 D821 S817 D824 S809 D827 S807
D826 S805
D816

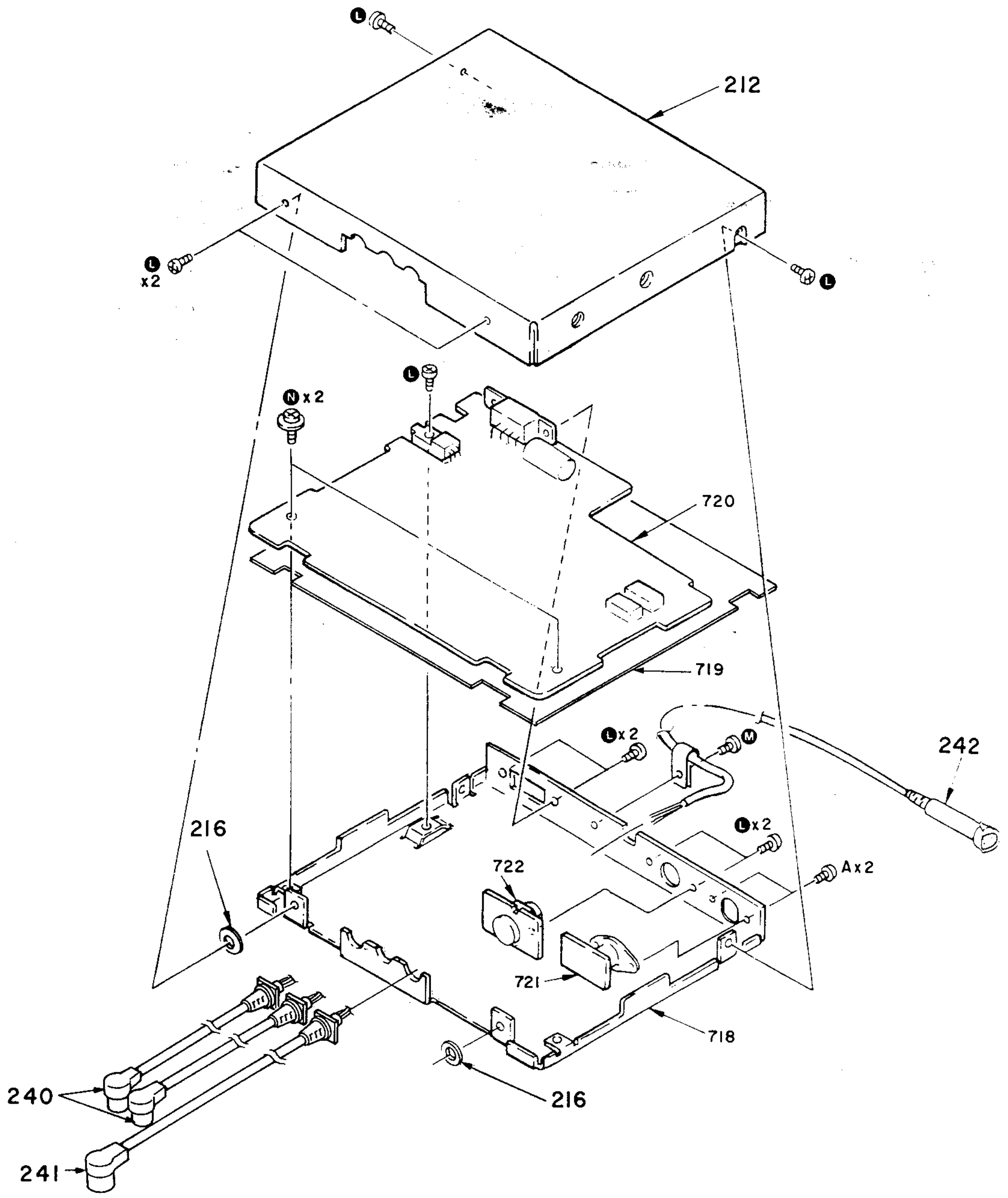
2

3

KDC-C100
(CONTROLLER)

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)

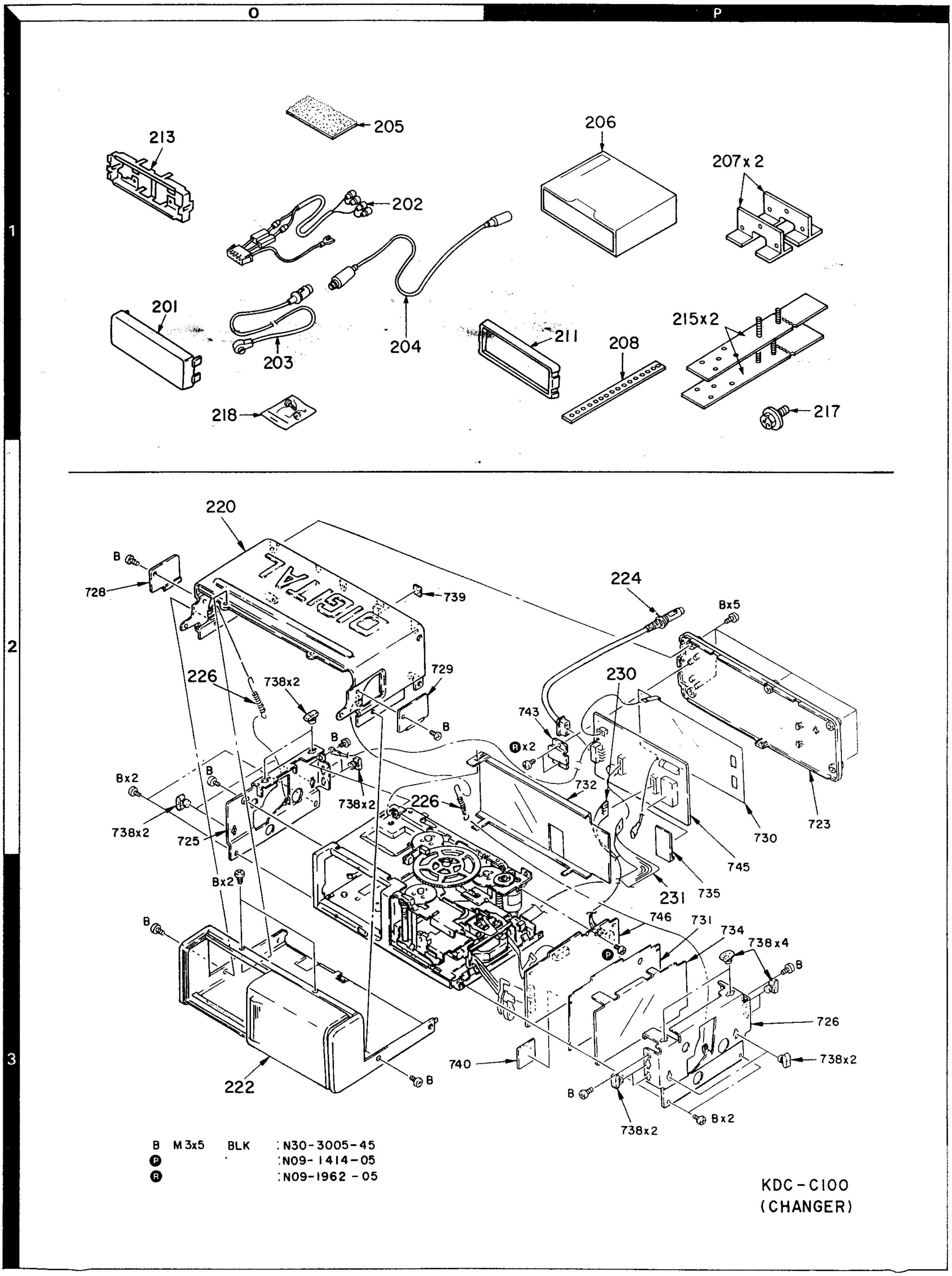

Ⓛ
212
Ⓛ x2
Ⓛ
Ⓛ
Ⓝ x2
720
719
Ⓛ x2
Ⓜ
242
216
722
Ⓛ x2
A x2
721
718
216
240
241

Ⓛ : N09-0395-05
Ⓜ : N09-1337-05
Ⓝ : N09-2623-08
A M2x6 : N30-2006-46

KDC-C100
(HIDE-AWAY)

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)


O
P
1
2
3
213
205
206
207x2
202
201
203
204
211
208
215x2
218
217
220
B
728
739
224
Bx5
226
738x2
729
230
743
Ⓡx2
B
Bx2
B
738x2
226
732
738x2
725
723
730
745
231
735
Bx2
B
746
731
734
738x4
Ⓟ
B
726
738x2
740
B
B
222
738x2
Bx2
KDC-C100
(CHANGER)

B M3x5 BLK : N30-3005-45
Ⓟ : N09-1414-05
Ⓡ : N09-1962-05

KDC-C100
(CHANGER)

Parts with the exploded numbers larger than 700 are not supplied

KDC-C100

PARTS LIST

⁎ New Parts

Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
				KDC-C100		
201	1O	⁎	B07-1886-08	PANEL FRAME (CONT/HIDE-AWAY)		
--			B46-0100-10	WARRANTY CARD		
--		⁎	B50-9068-00	INSTRUCTION MANUAL		
--		⁎	B58-0881-04	CAUTION CARD		
202	1O	⁎	E30-2430-05	POWER CONNECTION CORD		
203	1O	⁎	E30-2505-08	EXTENSION CORD (CONTROLLER)		
204	1O	⁎	E30-2506-08	EXTENSION CORD (CHANGER)		
205	1O	⁎	H30-0067-08	MAGIC TAPE		
--		⁎	H01-8315-08	ITEM CARTON BOX(CHANGER)		
--		⁎	H01-8316-08	ITEM CARTON BOX(CONT/HIDE-AWAY	KM	
--		⁎	H01-8343-08	ITEM CARTON BOX(CONT/HIDE-AWAY	ET	
--		⁎	H03-1417-08	OUTER PACKING CASE		
--		⁎	H10-3767-08	POLYSTYRENE FOAMED FIXTURE(BOT		
--		⁎	H10-3768-08	POLYSTYRENE FOAMED FIXTURE(UPP		
--		⁎	H10-3769-08	POLYSTYRENE FOAMED FIXTURE(BOT		
--		⁎	H11-0026-08	POLYSTYRENE FOAMED BOARD		
206	1P	⁎	J19-3101-08	DISC MAGAZINE		
207	1P	⁎	J19-3174-08	MOUNTING FITTING (CHANGER)		
208	1P	⁎	J21-5409-08	METAL MOUNTING STRAP		
211	1O	⁎	F07-0556-08	PROTECTION PANEL(CONT/HIDE-AWA		
213	1O	⁎	J21-5461-08	MOUNTING METAL FITTING(CONT/HI		
215	1P	⁎	J21-5462-08	MOUNTING PLATE (CHANGER)		
217	1P	⁎	N09-2683-08	SCREW (M4X6)		
218	1O	⁎	N99-0285-08	SCREW SET		
				CONTROLLER SECTION		
235	3K	⁎	A20-5664-08	PANEL ASSY	KM	
235	3K	⁎	A20-5665-08	PANEL ASSY	ET	
ND801	2K,2L	⁎	B38-0116-08	DISPLAY ASSY		
236	2L	⁎	E30-2480-08	CORD WITH CONNECTOR		
209	2K	⁎	K25-0011-08	KNOB (S816)		
J	2L	⁎	N09-2621-08	SCREW (Ø2X4)		
K	2L	⁎	N09-2622-08	SCREW (Ø2.6X10)		
BZ801	2L	⁎	T95-0106-08	PIEZOELECTRIC VIBRATOR		
240	1K	⁎	W03-2784-08	CONTROLLER ASSY	KM	
240	1K	⁎	W03-2785-08	CONTROLLER ASSY	ET	
				HIDE-AWAY SECTION		
212	1N	⁎	A01-1709-08	METALLIC CABINET(UPPER)		
240	3M	⁎	E30-2428-05	CORD WITH DIN CONNECTOR(OUTPUT		
241	3M	⁎	E30-2426-05	CORD WITH DIN CONNECTOR(AUX IN		
242	2N	⁎	E30-2481-08	CORD WITH CONNECTOR		
216	2M	⁎	N19-1180-08	FLAT WASHER		
L	1M,1N		N09-0395-05	SCREW (Ø3X6)		
M	2N		N09-1337-05	SCREW (Ø3X5)		
N	2M	⁎	N09-2623-08	SCREW(TP) (M3X5)		

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CHANGER SECTION						
220	1O	*	A01-1711-08	METALLIC CABINET		
222	3O	*	A21-1754-08	DRESSING PANEL		
224	1P	*	E30-2479-08	CORD WITH CONNECTOR		
226	2O	*	G01-2317-08	TENSION SP		
230	2P	*	J25-6030-08	FLEXIBLE BOARD (RF)		
231	2P	*	J25-6031-08	FLEXIBLE BOARD (ELV)		
P	3P		N09-1414-05	SCREW (Ø2.6X5)		
R	2P		N09-1962-05	SCREW (Ø2.6X6)		
ELECTRIC CIRCUIT MODULE (CONTROLLER SECTION)						
D805-810		*	B30-1251-08	LED		
D811		*	B30-1252-08	LED		
D812-831		*	B30-1251-08	LED		
D832		*	B30-1253-08	LED BLOCK		
C801			C92-0505-05	TANTAL 10UF 16WV		
C802			C92-0005-05	CHIP-TAN 2.2UF 6.3WV		
C803,804			C92-0505-05	TANTAL 10UF 16WV		
C806			CK73EB1H223K	CHIP C 0.022UF K		
C807		*	C92-0051-08	ELECTRO 47UF 10WV		
C808			CC41DSL1H220J	CYLND CHIP C 22PF J		
C809			CC41DSL1H100J	CYLND CHIP C 10PF J		
X801			L78-0251-08	RESONATOR		
R801			RK73EB2B102J	CHIP R 1.0K J 1/8W		
R802-807			RK73EB2B103J	CHIP R 10K J 1/8W		
R808			RK73EB2B221J	CHIP R 220 J 1/8W		
R809-817			RK73EB2B561J	CHIP R 560 J 1/8W		
S801-815		*	S59-1086-08	SWITCH		
S817,818		*	S59-1086-08	SWITCH		
D801			RD5.6ES(B2)	ZENER DIODE		
D802,803			1SS119	DIODE		
D804		*	B30-1254-08	LED (ATT/SDK)		
IC801		*	TC4050BF	IC(BUFFER/CONVERTER X6)		
IC802		*	75308GF-017-3B9	IC(MICROPROCESSOR)		
Q801		*	2SD1622	TRANSISTOR		
Q802,803			DTC114EK	DIGITAL TRANSISTOR		
ELECTRIC CIRCUIT MODULE (HIDE-AWAY SECTION)						
C101			CE04NW1C100M	ELECTRO 10UF 16WV		
C102		*	CE04NW1C010M	ELECTRO 1.0UF 16WV		
C103			CC41DSL1H100J	CYLND CHIP C 10PF J		
C104			CE04NW1C100M	ELECTRO 10UF 16WV		
C105		*	CK73FE1E334Z	CHIP C 0.33UF Z		
C107		*	C90-1735-08	ELECTRO 1000UF 6.3WV		
C108,109			CE04NW1C100M	ELECTRO 10UF 16WV		
C110			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C111			CE04NW1A330M	ELECTRO 33UF 10WV		
C112			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C113,114			CF92V1H333J	MF 0.033UF J		
C115			CK41DX1C332M	CYLND CHIP C 3300PF M		
C116			CK41DY1C103M	CYLND CHIP C 0.010UF M		

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C117			CC41DSL1H270J	CYLND CHIP C 27PF J		
C118,119			CE04NW1C100M	ELECTRO 10UF 16WV		
C120,121			CE04NW1C220M	ELECTRO 22UF 16WV		
C122			CK73EF1C105Z	CHIP C 1.0UF Z		
C125,126		*	CK41DB1H750K	CYLND CHIP C 75PF K		
C201			CE04NW1C100M	ELECTRO 10UF 16WV		
C202			CE04NW1H010M	ELECTRO 1.0UF 50WV		
C203			CC41DSL1H100J	CYLND CHIP C 10PF J		
C204			CE04NW1C100M	ELECTRO 10UF 16WV		
C205			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C207		*	C90-1735-08	ELECTRO 1000UF 6.3WV		
C208,209			CE04NW1C100M	ELECTRO 10UF 16WV		
C211			CE04NW1A330M	ELECTRO 33UF 10WV		
C213,214			CF92V1H333J	MF 0.033UF J		
C215			CK41DX1C332M	CYLND CHIP C 3300PF M		
C216			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C217			CC41DSL1H270J	CYLND CHIP C 27PF J		
C218,219			CE04NW1C100M	ELECTRO 10UF 16WV		
C220,221			CE04NW1C220M	ELECTRO 22UF 16WV		
C225,226		*	CK41DB1H750K	CYLND CHIP C 75PF K		
C301			CE04NW1C470M	ELECTRO 47UF 16WV		
C302			CE04NW1A470M	ELECTRO 47UF 10WV		
C303			CK73EB1E563K	CHIP C 0.056UF K		
C304			CE04NW1H0R1M	ELECTRO 0.1UF 50WV		
C305			CE04NW1A330M	ELECTRO 33UF 10WV		
C306			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C307		*	C90-1736-08	ELECTRO 0.22F 5.5WV		
C308			CE04NW1A221M	ELECTRO 220UF 10WV		
C309			CE04NW1A330M	ELECTRO 33UF 10WV		
C310			CK41DB1H471K	CYLND CHIP C 470PF K		
C311			C90-1263-05	ELECTRO 100UF 16WV		
C312			CE04NW1A470M	ELECTRO 47UF 10WV		
C313		*	C90-1733-08	ELECTRO 3300UF 16WV		
C314,315			CK73EB1E563K	CHIP C 0.056UF K		
C320			CE04NW1C330M	ELECTRO 33UF 16WV		
C323			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C324,325			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C329			CE04NW1C100M	ELECTRO 10UF 16WV		
C330			CE04NW1HR22M	ELECTRO 0.22UF 50WV		
C401			CK41DB1H471K	CYLND CHIP C 470PF K		
CT1		*	L33-0357-08	CHOKE COIL		
X301		*	L78-0252-08	RESONATOR		
R1 -4			RD41DB2B332J	CYLND CHIP R 3.3K J 1/8W		
R5			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R6 -10			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R11 ,12			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R13			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R14			RD41DB2B272J	CYLND CHIP R 2.7K J 1/8W		
R15			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R16			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R17 ,18			RD41DB2B432J	CYLND CHIP R 4.3K J 1/8W		
R19 ,20			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R101			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R102-105			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		

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R106			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R108			RD41DB2B913J	CYLND CHIP R 91K J 1/8W		
R109			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R110			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R111			RD41DB2B913J	CYLND CHIP R 91K J 1/8W		
R112			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R113			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R114			RD41DB2B123J	CYLND CHIP R 12K J 1/8W		
R115			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R116			RD41DB2B123J	CYLND CHIP R 12K J 1/8W		
R117			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R118			RD41DB2B122J	CYLND CHIP R 1.2K J 1/8W		
R119			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R120			RD41DB2B122J	CYLND CHIP R 1.2K J 1/8W		
R121			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R122			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R124			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R126			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R127			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R128			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R201			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R202-205			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R208			RD41DB2B913J	CYLND CHIP R 91K J 1/8W		
R209			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R210			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R211			RD41DB2B913J	CYLND CHIP R 91K J 1/8W		
R212			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R213			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R214			RD41DB2B123J	CYLND CHIP R 12K J 1/8W		
R215			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R216			RD41DB2B123J	CYLND CHIP R 12K J 1/8W		
R217			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R218			RD41DB2B122J	CYLND CHIP R 1.2K J 1/8W		
R219			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R220			RD41DB2B122J	CYLND CHIP R 1.2K J 1/8W		
R221			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R222			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R224			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R226			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R227			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R228			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R301,302			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R303			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R313			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R317			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R325			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R326			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R329			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R330			RD41DB2B391J	CYLND CHIP R 390 J 1/8W		
R331,332			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R334			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R337			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R338			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R340			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R341			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		

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R342			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R351			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R354			RD41DB2B101J	CYLND CHIP R 100 J 1/8W	ET	
R354			R92-0670-05	CHIP R 0 OHM	KM	
R357			RD41DB2B473J	CYLND CHIP R 47K J 1/8W	ET	
R358			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R360			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R361,362			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R366,367			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R401			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R402			RD41DB2B101J	CYLND CHIP R 100 J 1/8W		
R407			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W	ET	
R408			RD41DB2B103J	CYLND CHIP R 10K J 1/8W	ET	
RY301,302		*	S51-2086-08	RELAY		
D1		*	RD4.3ES(B1)	ZENER DIODE		
D2			1SS119	DIODE		
D3			RD5.1ES(B2)	ZENER DIODE		
D4			1SS119	DIODE		
D301			1SS119	DIODE		
D302		*	RD9.1ES(B2)	ZENER DIODE		
D303,304		*	DSA1A2	DIODE		
D307,308			RD5.1ES(B2)	ZENER DIODE		
D310,311			RD6.8ES(B2)	ZENER DIODE		
D313			1SS119	DIODE		
D314		*	RD6.2ES(B1)	ZENER DIODE		
D323		*	RD9.1ES(B2)	ZENER DIODE		
D324,325			1SS119	DIODE		
D327			1SS119	DIODE		
D328			RD5.1ES(B2)	ZENER DIODE		
IC101,102		*	LA6462M	IC(OP AMP X2)		
IC201,202		*	LA6462M	IC(OP AMP X2)		
IC301		*	LA6462M	IC(OP AMP X2)		
IC302		*	LC7537AN	IC(VOLUME,TONE)		
IC303		*	LA6462M	IC(OP AMP X2)		
IC304			S-8054HN-CB	IC(VOLTAGE DETECTOR)		
IC305		*	75106G-RMX2VF	IC(MICROPROCESSOR)		
IC306			S-8054HN-CB	IC(VOLTAGE DETECTOR)		
Q101,102		*	DTC343TS	DIGITAL TRANSISTOR		
Q201,202		*	DTC343TS	DIGITAL TRANSISTOR		
Q301-303			DTC114ES	DIGITAL TRANSISTOR		
Q304		*	2SD1388	TRANSISTOR		
Q305			DTC114ES	DIGITAL TRANSISTOR		
Q306			DTA114ES	DIGITAL TRANSISTOR		
Q307			DTC114ES	DIGITAL TRANSISTOR		
Q310			DTC114ES	DIGITAL TRANSISTOR		
Q311			2SB1202	TRANSISTOR		
Q312			DTC114ES	DIGITAL TRANSISTOR		
Q313		*	2SB733	TRANSISTOR		
Q314		*	2SD1388	TRANSISTOR		
Q315			DTA143XS	DIGITAL TRANSISTOR		
Q316			DTC124ES	DIGITAL TRANSISTOR		
Q319			2SC3851	TRANSISTOR		
Q401			DTC114ES	DIGITAL TRANSISTOR	ET	

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ELECTRIC CIRCUIT MODULE (CHANGER SECTION)						
C1			CF92V1H333J	MF 0.033UF J		
C2			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C3			CK73EB1H333K	CHIP C 0.033UF K		
C4			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C5			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C6			CE04NW0J470M	ELECTRO 47UF 6.3WV		
C7			CE04NW0J331M	ELECTRO 330UF 6.3WV		
C8			CK73EB1H183K	CHIP C 0.018UF K		
C9			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C10			CE04NW1HR47M	ELECTRO 0.47UF 50WV		
C11			CK41DY1C103M	CYLND CHIP C 0.010UF M		
C12			CK73EB1H183K	CHIP C 0.018UF K		
C13			CK41DX1C222M	CYLND CHIP C 2200PF M		
C14 ,15			CF92V1H104J	MF 0.10UF J		
C16			CE04NW0J331M	ELECTRO 330UF 6.3WV		
C17			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C18			CK41DB1H101K	CYLND CHIP C 100PF K		
C19			CE04NW1V3R3M	ELECTRO 3.3UF 35WV		
C20 ,21			CF92V1H104J	MF 0.10UF J		
C22			CK41DB1H101K	CYLND CHIP C 100PF K		
C23			CF92V1H104J	MF 0.10UF J		
C24			CF92V1H563J	MF 0.056UF J		
C25			CE04NW1H2R2M	ELECTRO 2.2UF 50WV		
C26			CK73EB1E683K	CHIP C 0.068UF K		
C27 ,28			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C29		*	CE04NW0J100M	ELECTRO 10UF 6.3WV		
C30			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C31			CK41DX1C472M	CYLND CHIP C 4700PF M		
C32			CK73EB1H333K	CHIP C 0.033UF K		
C33			CE04NW1HR47M	ELECTRO 0.47UF 50WV		
C34			CE04NW0J470M	ELECTRO 47UF 6.3WV		
C35			CK41DB1H102K	CYLND CHIP C 1000PF K		
C37 ,38			CE04NW1H010M	ELECTRO 1.0UF 50WV		
C39		*	CE04NW0J100M	ELECTRO 10UF 6.3WV		
C40 ,41			CC41DSL1H330J	CYLND CHIP C 33PF J		
C47			CK41DB1H102K	CYLND CHIP C 1000PF K		
C48			CE04NW0J331M	ELECTRO 330UF 6.3WV		
C49			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C50		*	CE04NW0J100M	ELECTRO 10UF 6.3WV		
C51 ,52		*	C90-1730-08	ELECTRO 1200UF 6.3WV		
C53			CE04NW0J331M	ELECTRO 330UF 6.3WV		
C54			CC41DSL1H200J	CYLND CHIP C 20PF J		
C55 ,56		*	CC41DSL1H4R7J	CYLND CHIP C 4.7PF J		
C57			CK73EB1E104K	CHIP C 0.10UF K		
C58			CE04NW1H010M	ELECTRO 1.0UF 50WV		
C101			CF92V1H104J	MF 0.10UF J		
C102,103			CK41DB1H102K	CYLND CHIP C 1000PF K		
C104			CK41DB1H820K	CYLND CHIP C 82PF K		
C105			CF92V1H683J	MF 0.068UF J		
C106,107			CE04NW1C100M	ELECTRO 10UF 16WV		
C201			CF92V1H104J	MF 0.10UF J		
C202,203			CK41DB1H102K	CYLND CHIP C 1000PF K		
C204			CK41DB1H820K	CYLND CHIP C 82PF K		

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C205			CF92V1H683J	MF 0.068UF J		
C206,207			CE04NW1C100M	ELECTRO 10UF 16WV		
C301			CE04NW0J331M	ELECTRO 330UF 6.3WV		
C302-305			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C501,502			CF92V1H104J	MF 0.10UF J		
C503			C90-1263-05	ELECTRO 100UF 16WV		
C505			CK41DX1C472M	CYLND CHIP C 4700PF M		
C506			CE04NW1C100M	ELECTRO 10UF 16WV		
C507			CE04NW0J101M	ELECTRO 100UF 6.3WV		
C508			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C511			CE04NW1H010M	ELECTRO 1.0UF 50WV		
C512			CE04NW1HR47M	ELECTRO 0.47UF 50WV		
C513			CF92V1H104J	MF 0.10UF J		
C542			C90-1263-05	ELECTRO 100UF 16WV		
C543			CF92V1H104J	MF 0.10UF J		
C546			CE04NW1C100M	ELECTRO 10UF 16WV		
C547		*	C90-1736-08	ELECTRO 0.22F 5.5WV		
C548			CF92V1H104J	MF 0.10UF J		
C549		*	CE04NW0J330M	ELECTRO 33UF 6.3WV		
C551			CK73EB1H102K	CHIP C 1000PF K		
C552			CF92V1H104J	MF 0.10UF J		
C703			CE04NW1H010M	ELECTRO 1.0UF 50WV		
C705			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
C706,707		*	C90-1731-08	ELECTRO 560UF 6.3WV		
C710		*	C90-1732-08	ELECTRO 330UF 16WV		
C718			CE04NW1C100M	ELECTRO 10UF 16WV		
C719		*	CE04NW0J330M	ELECTRO 33UF 6.3WV		
C720		*	C90-1733-08	ELECTRO 3300UF 16WV		
C721			CK41DF1E223Z	CYLND CHIP C 0.022UF Z		
CNJ4		*	E10-1817-08	CONNECTOR		
CNJ502		*	E10-1817-08	CONNECTOR		
CNJ503		*	E10-1817-08	CONNECTOR		
L1 -3		*	L39-0167-08	COIL		
L4		*	L39-0168-08	COIL		
L7		*	L39-0169-08	COIL		
L501		*	L39-0167-08	COIL		
L504-507		*	L39-0167-08	COIL		
X2			L77-1133-08	CRYSTAL RESONATOR		
X501		*	L78-0250-08	RESONATOR		
JW550			R92-0338-05	CLYND CHIP R 0 OHM		
R1			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R2			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R3 ,4		*	RD41DB2B110J	CYLND CHIP R 11 J 1/8W		
R5			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R6			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R7			RD41DB2B133J	CYLND CHIP R 13K J 1/8W		
R8			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R9			RD41DB2B113J	CYLND CHIP R 11K J 1/8W		
R10			RD41DB2B474J	CYLND CHIP R 470K J 1/8W		
R11			RD41DB2B154J	CYLND CHIP R 150K J 1/8W		
R12 ,13			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R14			RD41DB2B334J	CYLND CHIP R 330K J 1/8W		
R15			RD41DB2B683J	CYLND CHIP R 68K J 1/8W		
R16			RD41DB2B124J	CYLND CHIP R 120K J 1/8W		

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R17			RD41DB2B514J	CYLND CHIP R 510K J 1/8W		
R18			RD41DB2B822J	CYLND CHIP R 8.2K J 1/8W		
R19			RD41DB2B274J	CYLND CHIP R 270K J 1/8W		
R20			RD41DB2B683J	CYLND CHIP R 68K J 1/8W		
R21			RD41DB2B332J	CYLND CHIP R 3.3K J 1/8W		
R22			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R23			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R24			RD41DB2B203J	CYLND CHIP R 20K J 1/8W		
R25			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R27			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R28			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R29			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R38			RD41DB2B243J	CYLND CHIP R 24K J 1/8W		
R39			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R40			RD41DB2B910J	CYLND CHIP R 91 J 1/8W		
R50			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R51			RD41DB2B3R3J	CYLND CHIP R 3.3 J 1/8W		
R52			RD41DB2B153J	CYLND CHIP R 15K J 1/8W		
R53			RD41DB2B3R3J	CYLND CHIP R 3.3 J 1/8W		
R54			RD41DB2B100J	CYLND CHIP R 10 J 1/8W		
R55 ,56			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R58			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R100			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R101		*	R92-0376-08	CYLND CHIP R 5.6K J 1/8W		
R102			RD41DB2B562J	CYLND CHIP R 5.6K J 1/8W		
R103			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R104			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R105			RD41DB2B153J	CYLND CHIP R 15K J 1/8W		
R106			RD41DB2B471J	CYLND CHIP R 470 J 1/8W		
R107			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R108			RD41DB2B181J	CYLND CHIP R 180 J 1/8W		
R109			RD41DB2B474J	CYLND CHIP R 470K J 1/8W		
R110,111			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R112			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R200			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R201		*	R92-0376-08	CYLND CHIP R 5.6K J 1/8W		
R202			RD41DB2B562J	CYLND CHIP R 5.6K J 1/8W		
R203			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R204			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R205			RD41DB2B153J	CYLND CHIP R 15K J 1/8W		
R206			RD41DB2B471J	CYLND CHIP R 470 J 1/8W		
R207			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R208			RD41DB2B181J	CYLND CHIP R 180 J 1/8W		
R209			RD41DB2B474J	CYLND CHIP R 470K J 1/8W		
R210,211			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R212			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R301			RD41DB2B391J	CYLND CHIP R 390 J 1/8W		
R303,304			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R305,306			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R401-404			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R503			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R505			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R506			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R507,508			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R516			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		

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R518-521			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R530			RD41DB2B221J	CYLND CHIP R 220 J 1/8W		
R531			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R532			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R533-537			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R540			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R541,542			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R704			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R705			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R706			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R707			RD41DB2B471J	CYLND CHIP R 470 J 1/8W		
R708			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R709			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R710			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R711			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R713		*	RD14DB2H1R0J	SMALL-RD 1.0 J 1/2W		
RV1			R12-3097-05	TRIMMING POT.(22K)TR OFFSET		
RV2			R12-3099-05	TRIMMING POT.(47K)FOCUS OFFSET		
RV3 ,4			R12-3097-05	TRIMMING POT.(22K)F/G,T/G		
RV5			R12-1067-05	TRIMMING POT.(2.2K)VCO		
SW101		*	S59-1085-08	KEY BOARD SWITCH(EJECT)		
SW102		*	S50-1050-08	MICRO SWITCH (CBP)		
SW103		*	S50-1051-08	MICRO SWITCH (M1)		
SW104		*	S50-1052-08	MICRO SWITCH (HOME)		
D1			DLS1585	DIODE		
D301			DLS1585	DIODE		
D302			1S2837	DIODE		
D401,402			TLR123	LED		
D403-405			1S2835	DIODE		
D501		*	RD9.1ES(B1)	ZENER DIODE		
D502			RD5.1ES(B2)	ZENER DIODE		
D503			1S2835	DIODE		
D505			1S2835	DIODE		
D507			RD5.1ES(B2)	ZENER DIODE		
D508			1SS119	DIODE		
D509			RD13ES(B1)	ZENER DIODE		
D511-515			RD5.1ES(B2)	ZENER DIODE		
D518			1SS119	DIODE		
D703			DLS1585	DIODE		
D704			HZ6A2L	DIODE		
D705			RD6.2E(B2)	ZENER DIODE		
D706			RD5.1ES(B2)	ZENER DIODE		
D707			RD18ES(B1)	ZENER DIODE		
D708			DLS1585	DIODE		
D709			RD5.1ES(B2)	ZENER DIODE		
D710			DLS1585	DIODE		
IC1			CXA1081Q	IC(SURVO SIGNAL PROCESSOR)		
IC2			CXA1082AQ	IC(SERVO SIGNAL PROCESSOR)		
IC3			CXD1130Q	IC(DIGITAL SIGNAL PROCESSOR)		
IC4		*	MB88505H-657M	IC(MICROPROCESSOR)		
IC5			L272M	IC(MOTOR DRIVE)		
IC6		*	CXK5816M-10L	IC(2K BYTE X8 RAM (CMOS))		
IC301		*	CXD1161M-2	IC(D/A CONVERTER)		
IC302,303		*	LA6462M	IC(OP AMP X2)		

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IC501			LB1649	IC(MOTOR DRIVER)		
IC502			S-8054HN-CB	IC(VOLTAGE DETECTOR)		
IC503		*	CX-7991	IC(PORT EXPANDER)		
IC505		*	7508HG-593-22	IC(MICROPROCESSOR)		
IC507			LB1649	IC(MOTOR DRIVER)		
Q1 ,2			2SB1122	TRANSISTOR		
Q3		*	2SD1622	TRANSISTOR		
Q4			2SB1122	TRANSISTOR		
Q5		*	2SD1622	TRANSISTOR		
Q6			DTC124EK	DIGITAL TRANSISTOR		
Q8			2SC2712	TRANSISTOR		
Q9			DTC114EK	DIGITAL TRANSISTOR		
Q10			DTC144EK	DIGITAL TRANSISTOR		
Q101,102			2SC2878	TRANSISTOR		
Q201,202			2SC2878	TRANSISTOR		
Q301			DTA124EK	DIGITAL TRANSISTOR		
Q302			DTC124EK	DIGITAL TRANSISTOR		
Q303			DTA124EK	DIGITAL TRANSISTOR		
Q304			DTC124EK	DIGITAL TRANSISTOR		
Q401,402			PH102	PHOTO TRANSISTOR		
Q403		*	GP-1S03	PHOTO DETECTOR		
Q502			2SA1162(Y)	TRANSISTOR		
Q505,506			2SA1162(Y)	TRANSISTOR		
Q511			DTA124EK	DIGITAL TRANSISTOR		
Q512			DTC124EK	DIGITAL TRANSISTOR		
Q513			DTA124EK	DIGITAL TRANSISTOR		
Q514			2SC2712	TRANSISTOR		
Q515			DTA124EK	DIGITAL TRANSISTOR		
Q516			2SC2712	TRANSISTOR		
Q517			DTA124EK	DIGITAL TRANSISTOR		
Q518,519			DTC124EK	DIGITAL TRANSISTOR		
Q520			DTA124EK	DIGITAL TRANSISTOR		
Q523			2SC2712	TRANSISTOR		
Q524			DTA124EK	DIGITAL TRANSISTOR		
Q704			DTC124EK	DIGITAL TRANSISTOR		
Q705			2SB1202	TRANSISTOR		
Q706			2SC2412K	TRANSISTOR		
Q707		*	2SD1622	TRANSISTOR		
Q710			DTC114EK	DIGITAL TRANSISTOR		
TH1 ,2			ERT-D2FHJ802T	THERMISTOR		
THP501		*	PTH59F04BG222TS	THERMISTOR		
DD1		*	W02-0960-08	DC-DC CONVERTER		
			MECHANISM ASS'Y			
1	2D	*	A10-1877-08	CHASSIS ASSY		
2	2G	*	A10-1878-08	CHASSIS ASSY (PACK)		
3	2H	*	A10-1879-08	CHASSIS ASSY (BOTTOM)		
4	2A	*	A10-1880-08	CHASSIS ASSY		
5	2I		A13-1103-08	FRAME (MD SLED)		
6	2A	*	B07-1860-08	ESCUTCHEON		
8	2C	*	D10-2257-08	LEVER ASSY		
9	1D	*	D10-2258-08	LEVER (SLIDE)		
10	2E	*	D10-2259-08	LEVER ASSY (LINK)		
11	2F	*	D10-2260-08	LEVER ASSY (LINK)		

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12	3H	*	D10-2261-08	LEVER ASSY	(A)		
15	2H	*	D10-2262-08	LEVER ASSY	(B)		
16	2G	*	D10-2263-08	LEVER ASSY	(LINEAR)		
17	1G	*	D10-2264-08	LEVER ASSY	(SLIDER SET)		
18	2G	*	D10-2265-08	LEVER ASSY	(SOFT EJECT)		
19	2G	*	D10-2266-08	LEVER	(BACK LOCK HOOK)		
22	2G,2H	*	D10-2267-08	LEVER	(SOFT EJECT2)		
23	2E	*	D10-2268-08	LEVER	(DISC LINK)		
24	1G	*	D10-2269-08	SLIDER ASSY	(LINEAR)		
25	3I		D13-0671-08	GEAR	(B)		
26	2A	*	D13-0760-08	GEAR	(ELEVATOR)		
30	1A	*	D13-0761-08	GEAR	(ELEVATOR)		
31	1B	*	D13-0762-08	GEAR	(ELEVATOR)		
32	2B	*	D13-0763-08	GEAR	(MOTOR)		
33	2C	*	D13-0764-08	GEAR (E)			
34	1D	*	D13-0765-08	GEAR (F)			
35	2D	*	D13-0766-08	GEAR (A)			
36	2D	*	D13-0767-08	GEAR (B)			
37	1F	*	D13-0768-08	GEAR (G)	(ROLLER)		
38	2F	*	D13-0769-08	GEAR	(ROLLER STEP)		
39	2G	*	D13-0770-08	GEAR			
43	2G	*	D13-0771-08	GEAR	(WORM WHEEL)		
44	2G	*	D13-0772-08	GEAR ASSY			
45	2G,2H	*	D13-0773-08	GEAR	(EJECT CAM)		
46	2C,2E		D14-0269-08	ROLLER	(LOWER)		
50	2A	*	D14-0289-08	ROLLER	(MAGAZINE)		
51	1D	*	D14-0290-08	ROLLER	(IDEL)		
52	2E	*	D14-0291-08	ROLLER ASSY	(UPPER)		
53	2G	*	D14-0292-08	ROLLER (A)			
54	2G	*	D14-0293-08	ROLLER			
59	1G	*	D14-0295-08	ROLLER			
60	2I		D21-1437-08	SHAFT	(GUIDE)		
61	2A	*	D21-1506-08	SHAFT	(MAGAZINE)		
62	2C	*	D21-1507-08	SHAFT ASSY	(POLLER)		
65	2D	*	D21-1508-08	SHAFT	(DISC CHUCK)		
66	2F	*	D21-1509-08	SHAFT	(SIDE ROLLER)		
67	2F	*	D21-1510-08	SHAFT ASSY	(UPPER ROLLER)		
68	1G	*	D21-1511-08	SHAFT	(LINEAR SLIDER)		
69	3G	*	D21-1512-08	SHAFT	(LOCK HOOK)		
72	2H	*	D21-1513-08	SHAFT	(FIXED B)		
73	2H	*	D21-1514-08	SHAFT	(FIXED A)		
74	2I		D23-0232-08	RETAINER ASSY			
78	2J		D23-0233-08	RETAINER			
79	2I		D23-0234-08	RETAINER			
80	2A,2B		D23-0239-08	RETAINER			
81	2C		D23-0240-08	RETAINER	(MAIN ROLLER)		
82	2C	*	D23-0241-08	RETAINER			
84	2C	*	D29-0017-08	SCREW ASSY	(FEED)		
85	2E	*	D32-0182-08	STOPPER	(ROLLER)		
156	2I	*	E29-0331-08	LEAD PLATE			
90	2I		F07-0523-08	COVER			
91	3H	*	F20-1217-08	INSULATING SHEET			
92	1C	*	F31-0178-08	REINFORCING HARDWARE			

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95	2D	*	G01-2318-08	TENSION SP		
96	3D	*	G01-2319-08	TENSION SP		
97	2E,2F	*	G01-2320-08	TENSION SP		
98	1G	*	G01-2321-08	COMPRESSION SP		
99	2G	*	G01-2322-08	TENSION SP		
102	2G	*	G01-2323-08	TENSION SP		
103	2G	*	G01-2324-08	TENSION SP		
104	2C,2D	*	G01-2325-08	COMPRESSION SP		
106	2A	*	G02-0905-08	LEAF SPRING		
108	1A	*	G02-0906-08	LEAF SPRING		
109	1A	*	G02-0907-08	LEAF SPRING		
110	1A	*	G02-0908-08	LEAF SPRING		
111	2C	*	G02-0909-08	LEAF SPRING		
112	2H	*	G11-1315-08	CUSHION		
115	2B	*	G11-1323-08	CUSHION		
116	2C	*	G11-1323-08	CUSHION		
117	3H	*	G11-1323-08	CUSHION		
118	2D	*	G11-1324-08	CUSHION		
7	2A	*	J25-6174-08	PRINTED WIRING BOARD		
121	3D	*	J11-0138-08	CLAMPER		
122	2B	*	J11-0139-08	CLAMPER		
123	3B	*	J19-3102-08	BRACKET		
124	3D	*	J19-3103-08	BRACKET		
125	2H	*	J19-3104-08	BRACKET		
128	2C	*	J19-3105-08	BRACKET		
129	2C	*	J19-3106-08	HOLDER		
130	3D	*	J19-3107-08	HOLDER ASSY		
131	2J		J25-5830-08	PRINTED WIRING BOARD(FLEXIBLE)		
132	1A	*	J25-6041-08	PRINTED WIRING BOARD		
135	2C	*	J25-6042-08	PRINTED WIRING BOARD		
136	2C	*	J25-6043-08	PRINTED WIRING BOARD		
137	2C	*	J25-6044-08	PRINTED WIRING BOARD		
138	2D	*	J25-6045-08	PRINTED WIRING BOARD		
139	3C	*	J25-6046-08	PRINTED WIRING BOARD		
142	3D	*	J25-6047-08	PRINTED WIRING BOARD		
143	2H	*	J25-6048-08	PRINTED WIRING BOARD		
144	2G	*	J25-6049-08	PRINTED WIRING BOARD		
145	2G	*	J25-6050-08	PRINTED WIRING BOARD		
146	2G	*	J25-6051-08	PRINTED WIRING BOARD		
149	2H	*	J25-6052-08	PRINTED WIRING BOARD		
150	3H	*	J25-6053-08	PRINTED WIRING BOARD		
151	2J	*	J90-0634-08	GUIDE		
152	2F	*	J90-0628-08	GUIDE		
153	2J		J91-0346-08	PICK UP		
M2	3C	*	T42-0511-08	DC MOTOR ASSY		
155	2A	*	K24-0054-08	KNOB (EJECT)		
158	2C	*	N14-0185-08	NUT		
159	3I		N19-1120-08	FLAT WASHER		
160	2E	*	N19-1189-08	FLAT WASHER (0.5X5.5X2.1)		
161	2C	*	N19-1190-08	FLAT WASHER		
162	2D	*	N19-1192-08	FLAT WASHER		
163	2A		N24-3015-45	E TYPE RETAINING RING (Ø1.5)		

E: Scandinavia & Europe **K**: USA **P**: Canada
U: PX(Far East, Hawaii) **T**: England **M**: Other Areas
UE: AAFES(Europe) **X**: Australia

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
164	3D		N24-3015-45	E TYPE RETAINING RING (Ø1.5)		
165	3G		N24-3015-45	E TYPE RETAINING RING (Ø1.5)		
166	1F,2F		N24-3015-45	E TYPE RETAINING RING (Ø1.5)		
167	2D		N24-3020-45	E TYPE RETAINING RING (Ø2.0)		
168	2G		N24-3020-45	E TYPE RETAINING RING (Ø2.0)		
169	1B		N24-3025-45	E TYPE RETAINING RING		
A	2I		N09-1304-05	SCREW		
B	2I		N09-1936-08	SCREW		
C	3I		N09-1942-08	SCREW		
D	3I		N09-1943-08	SCREW		
E	1J		N09-1944-08	SCREW		
F	2B	*	N09-2639-08	SCREW		
S902	3J		S46-1107-08	LEAF SWITCH (LIMIT)		
SW105	2G	*	S50-1052-08	MICRO SWITCH (LOT)		
SW106	2G	*	S50-1052-08	MICRO SWITCH (PST)		
SW107	2G	*	S50-1052-08	MICRO SWITCH (EJECT)		
M1	2H	*	T42-0512-08	MOTOR ASSY		
M3	2B	*	T42-0510-08	DC MOTOR		
M902	2J		T43-0053-08	MOTOR ASSY		

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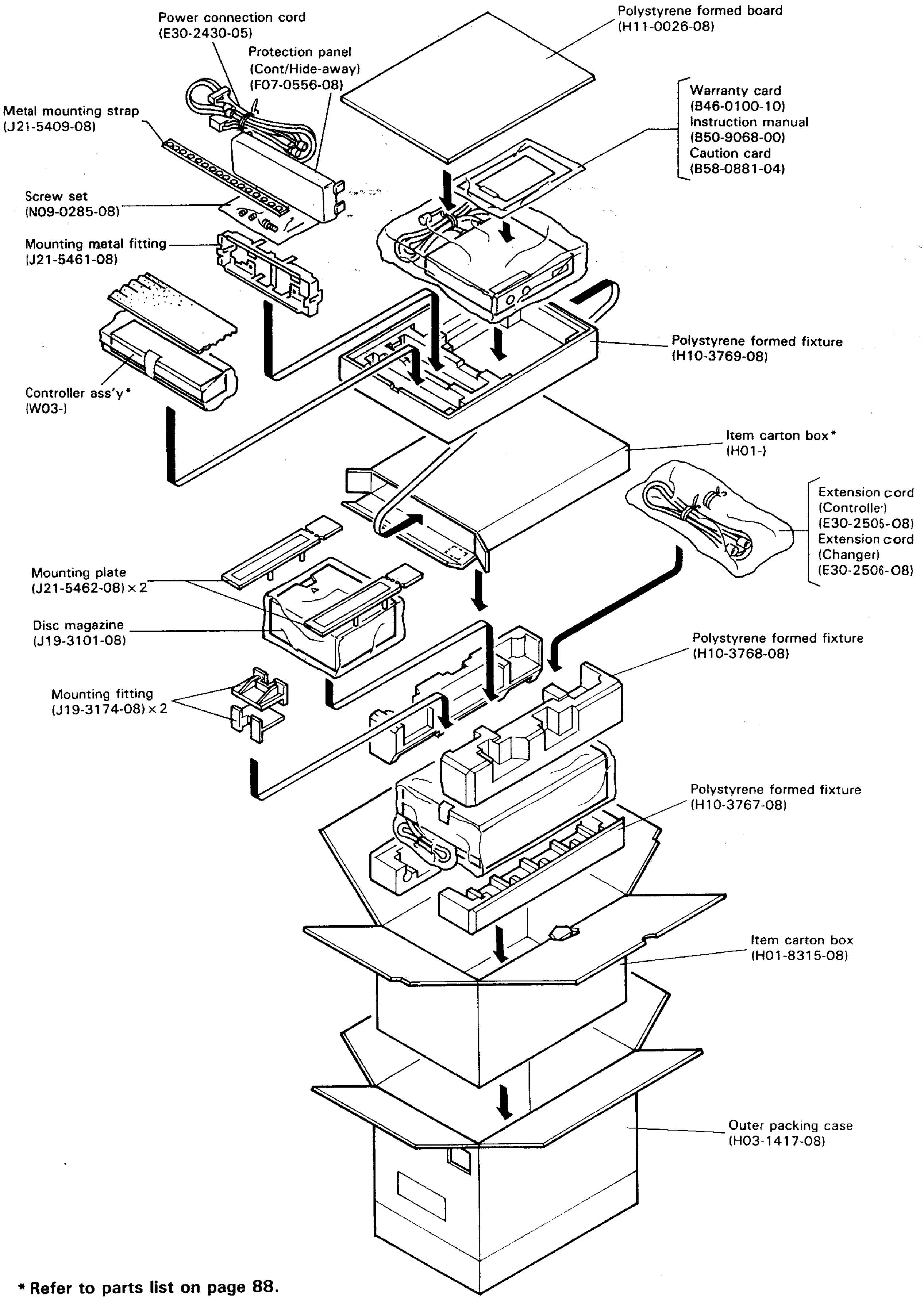
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PACKING


Power connection cord
(E30-2430-05)
Protection panel
(Cont/Hide-away)
(F07-0556-08)
Metal mounting strap
(J21-5409-08)
Screw set
(N09-0285-08)
Mounting metal fitting
(J21-5461-08)
Controller ass'y*
(W03-)
Polystyrene formed board
(H11-0026-08)
Warranty card
(B46-0100-10)
Instruction manual
(B50-9068-00)
Caution card
(B58-0881-04)
Polystyrene formed fixture
(H10-3769-08)
Item carton box*
(H01-)
Extension cord
(Controller)
(E30-2505-08)
Extension cord
(Changer)
(E30-2506-08)
Mounting plate
(J21-5462-08) x 2
Disc magazine
(J19-3101-08)
Mounting fitting
(J19-3174-08) x 2
Polystyrene formed fixture
(H10-3768-08)
Polystyrene formed fixture
(H10-3767-08)
Item carton box
(H01-8315-08)
Outer packing case
(H03-1417-08)

*** Refer to parts list on page 88.**

KDC-C100

SPECIFICATIONS

Disc Section

Laser Diode	GaAlAs (λ = 780 nm)
D-A Conversion	16 bit (Linear)
Sampling Frequency	44.1 kHz
Conversion Rate	88.2 kHz
Spindle Speed	500 ~ 200 rpm (CLV)
Wow & Flutter	Below Mesurable Limit
Frequency Response (± 1 dB)	5 Hz ~ 20 kHz
Total Harmonic Distortion (1 kHz)	0.005%
Signal to Noise Ratio	85 dB
Dynamic Range	85 dB
Channel Separation	85 dB
Laser Diode Properties	
Material	GaAlAs
Wavelength	780 nm
Emission Duration	Continuous
Laser Output Power	Less than 44.6 µW

* This output is the value measured at a distance of 200 mm from the objective lens surface on the Optical Pick-up Block.

Audio Section

Tone Action (BASS)	100 Hz ± 10 dB
(TREBLE)	10 kHz ± 10 dB
Preout Level	1.5 V

General

Operating Voltage	14.4 V (11 ~ 16 V)
Current Consumption	0.8 A
Operating Temperature	− 10 ~ 50 °C
Size (W × H × D)	
Controller	172 × 48 × 23 mm (6-3/4 × 1-7/8 × 7/8 in.)
Changer main unit	310 × 98 × 200 mm (11-7/8 × 3-7/8 × 7-7/8 in.)
Hide-away unit	178 × 25 × 135 mm (7 × 1 × 5-5/16 in.)
Weight	
Controller	0.3 kg (0.7 lb)
Changer main unit	3.0 kg (6.6 lb)
Hide away unit	0.7 kg (1.5 lb)

Kenwood follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Kenwood poursuit une politique de progrès constants en ce qui doncerne le développement. Pour cette raison, les spécifications sont sujettes à modifications sans préavis.

Kenwood strebt ständige, Verbesserungen in der Entwicklung an. Daher bleiben Änderungen der technischen Daten jederzeit vorbehalten.

Note:

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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